Texas Instruments

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SCOPE™

System Controllability/Observability Partitioning Environment

Product Information

Preliminary

October 1992

General Purpose Logic Products

SCOPE™
System Controllability/Observability Partitioning Environment Product Information

1992

TEXAS INSTRUMENTS

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INTRODUCTION

In addition to the popular JTAG/IEEE 1149.1 devices currently available in BiCMOS Technology (BCT), Texas Instruments now offers Advanced BiCMOS Technology (ABT). This state-of-the-art family was developed in response to customer demands for faster speeds, lower power consumption, and improved simultaneous switching performance for high-performance system applications. The new ABT JTAG devices offer all of these benefits plus the ability to enhance your time to market by allowing for reduced design verification and diagnostic time.

ABT is manufactured using a 0.8-micron BiCMOS process. A full selection of devices are offered including 8-, 18-, and 20-bit bus drivers, latches, registers, and registered transceivers. Features include:

- Compatibility with the JTAG/IEEE 1149.1 testability standard
- Typical propagation delays of < 4 ns
- Test extensions to support board-level built-in self test (BIST)
- State-of-the-art EPICIIB™ design that significantly reduces power dissipation
- 8-, 18-, and 20-bit functions
- High-drive outputs
- Variety of 24-, 28-, 56-, and 64-pin advanced packaging options

This information booklet provides pertinent technical information on existing and planned ABT JTAG logic devices. Additionally, similar information is provided for other testability devices that support boundary scan. These include devices for controlling the test bus, performing at-speed functional testing, partitioning long scan paths, and a *diary* memory device that is the industry's first memory device to support boundary scan.

Section 2 of the booklet contains a collection of customer presentations that address the following issues:

– TI's Advanced Support System for Emulation and Test (ASSET™)

– JTAG Widebus+™

For more information on the Texas Instruments JTAG/IEEE 1149.1 products, please contact your local TI field sales office or authorized distributor. You may direct specific questions concerning JTAG devices in this booklet to:

Johnny Young – GPL Testability Product Marketing Manager
(214) 997-5263

Adam Ley – GPL Member Technical Staff, Testability Applications Support
(903) 868-5761

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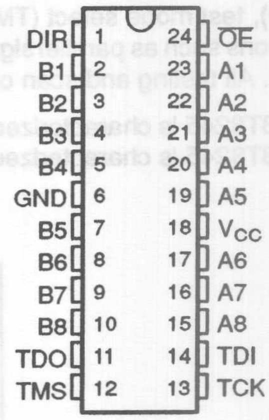
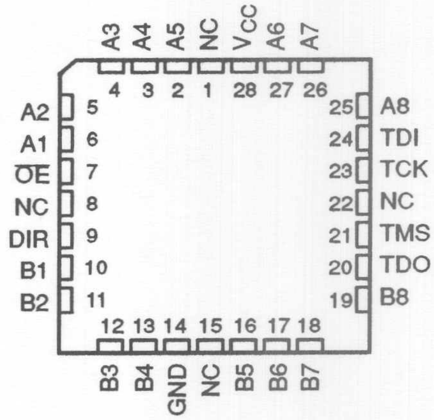
The information relating to the JTAG/IEEE 1149.1–1990 state diagram, instructions, and boundary control register opcodes is common to each of the data sheets for the ’ABT8245, ’ABT8543, ’ABT8646, ’ABT8652, and ’ABT8952. Therefore, this information is only shown for the ’ABT8245. To obtain these descriptions for the JTAG Widebus™ products, please contact your local TI sales representative.

- **Members of the Texas Instruments *SCOPE* ™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74F245 and SN54/74ABT245 in the Normal Function Mode**
- ***SCOPE* ™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPICIIB*™ BICMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8245 . . . JT PACKAGE
SN74ABT8245 . . . DB OR DW PACKAGE
(TOP VIEW)



SN54ABT8245 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54ABT8245 and SN74ABT8245 scan test devices with octal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F245 and SN54/74ABT245 octal bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

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On products compliant to MIL-STD-883, Class B, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

description (continued)

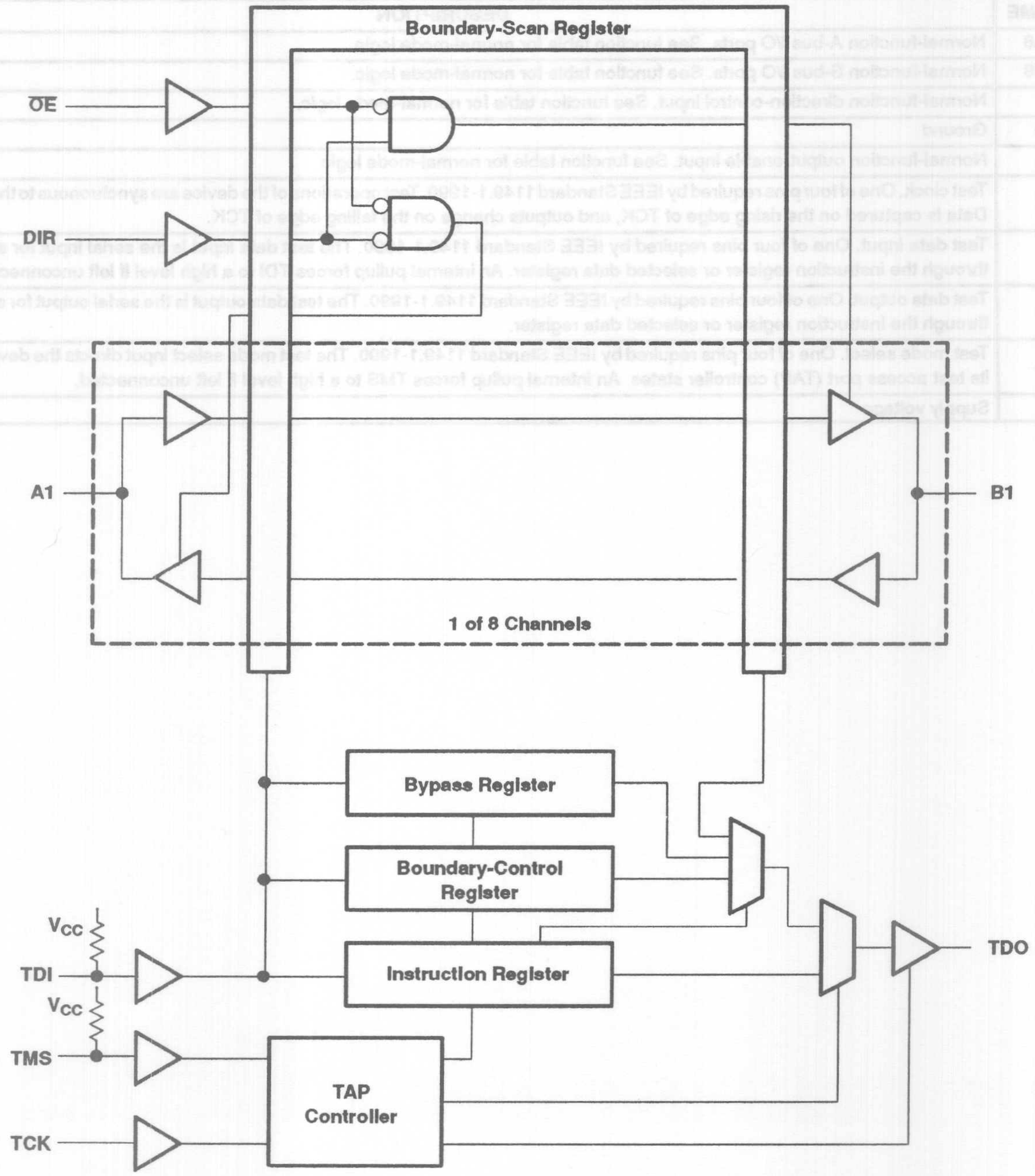
Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT8245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

functional block diagram



Terminal Functions

PIN NAME	DESCRIPTION
A1 – A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1 – B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
DIR	Normal-function direction-control input. See function table for normal-mode logic.
GND	Ground
$\overline{OE}$	Normal-function output-enable input. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

test architecture

Serial test information is conveyed by means of a 4-wire test bus, or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. NO TAG shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test data registers: a 36-bit boundary-scan register, an 11-bit boundary-control register, and a one-bit bypass register.

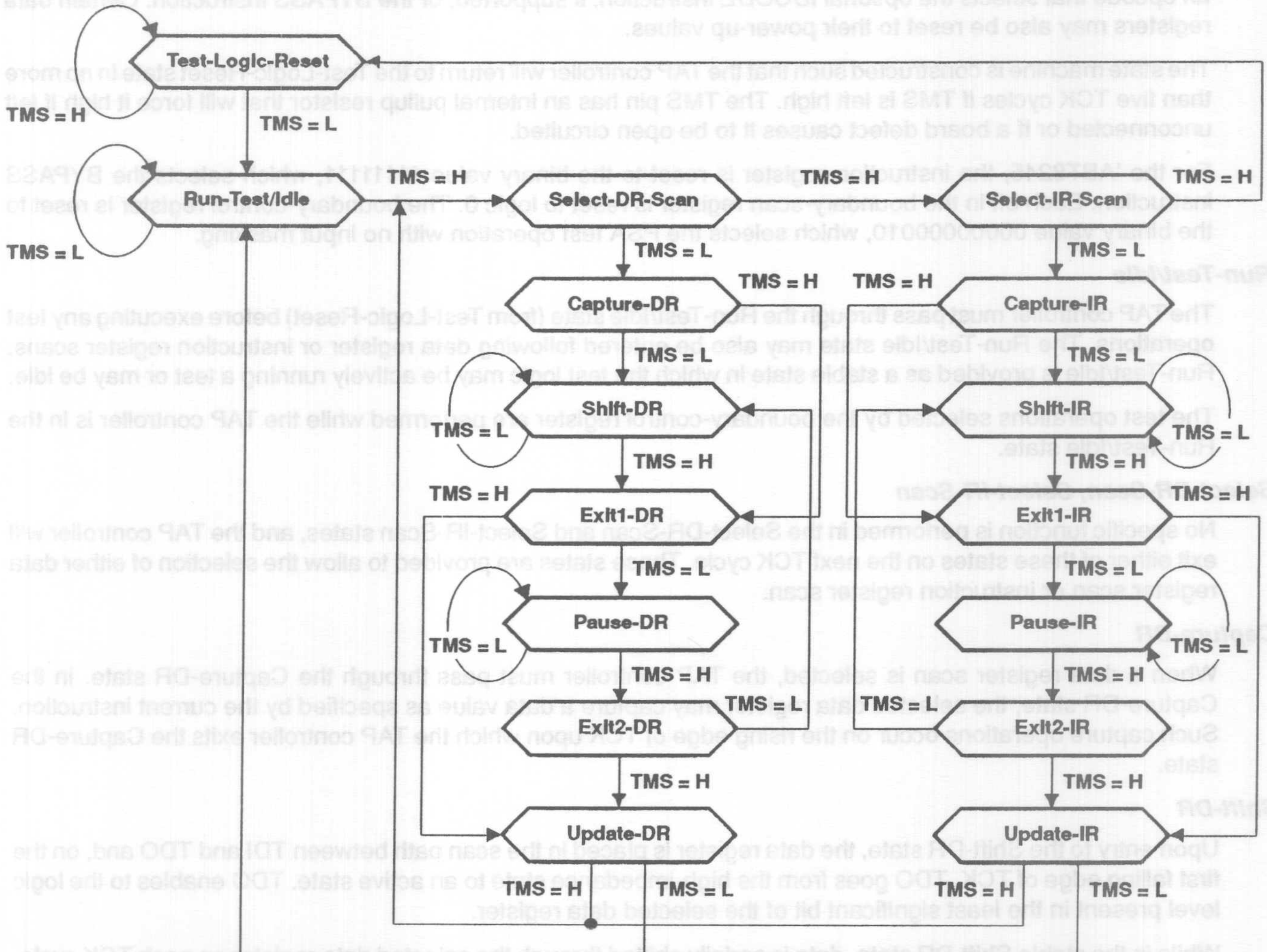


Figure 1. TAP Controller State Diagram

state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in NO TAG and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register may be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers may also be reset to their power-up values.

The state machine is constructed such that the TAP controller will return to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that will force it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8245, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 0000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state may also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic may be actively running a test or may be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller will exit either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register may capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

state diagram description (continued)

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT8245, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

With the exception of the bypass register, any test register may be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

NO TAG lists the instructions supported by the 'ABT8245. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

The instruction register order of scan is illustrated in Figure 2.

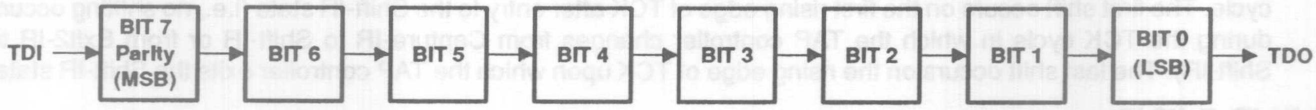


Figure 2. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 36 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, two BSCs for each normal-function I/O pin (one for input data and one for output data), and one BSC for each of the internally decoded output-enable signals (OEA and OEB). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR may change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals OEA and OEB capture logic values determined by the following positive-logic equations: $OEA = \overline{OE} \bullet \overline{DIR}$, and $OEB = \overline{OE} \bullet DIR$. When data is to be applied externally, these BSCs control the drive state (active or high-impedance) of their respective outputs.

The boundary-scan register order of scan is from TDI through bits 35–0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
35	OEB	31	B8-I	23	B8-O	15	A8-I	7	A8-O
34	OEA	30	B7-I	22	B7-O	14	A7-I	6	A7-O
33	DIR	29	B6-I	21	B6-O	13	A6-I	5	A6-O
32	$\overline{OE}$	28	B5-I	20	B5-O	12	A5-I	4	A5-O
—	—	27	B4-I	19	B4-O	11	A4-I	3	A4-O
—	—	26	B3-I	18	B3-O	10	A3-I	2	A3-O
—	—	25	B2-I	17	B2-O	9	A2-I	1	A2-O
—	—	24	B1-I	16	B1-O	8	A1-I	0	A1-O

boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA) with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The boundary-control register order of scan is from TDI through bits 10–0 to TDO. NO TAG shows the boundary-control register bits and their associated test control signals.

Table 2. Boundary-Control Register Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1	—	—

data register description (continued)

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0.

The bypass register order of scan is illustrated in Figure 3.

Figure 3. Bypass Register Order of Scan

Table 3. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary-scan	Test
10000001	BYPASS‡	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary-scan	Normal
00000011	INTEST	Boundary scan	Boundary-scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary-scan	Normal
10001011	READBT	Boundary read	Boundary-scan	Test
00001100	CELLTST	Boundary self test	Boundary-scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary-control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary-control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8245.

instruction register opcode description

The instruction register opcodes are shown in NO TAG. The following descriptions detail the operation of each instruction.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches may be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.

instruction register opcode description (continued)

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

Table 4. Boundary-Control Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/16-bit mode (PRPG)
X10	Parallel signature analysis/16-bit mode (PSA)
011	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

It should be noted, in general, that while the control input BSCs (bits 35–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 35–34 of the BSR) do control the drive state (active or high-impedance) of the selected device output pins. It also should be noted that these BCR instructions are only valid when the device is operating in one direction of data flow (that is, OEA ≠ OEB). Otherwise, the bypass instruction is operated.

PSA input masking

Bits 10–3 of the boundary-control register are used to specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in NO TAG. When the mask bit which corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

boundary-control register opcode description (continued)

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift register elements of the selected BSCs on each rising edge of TCK and then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK. This data is also updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Figures 4 and 5 illustrate the 16-bit linear-feedback shift register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

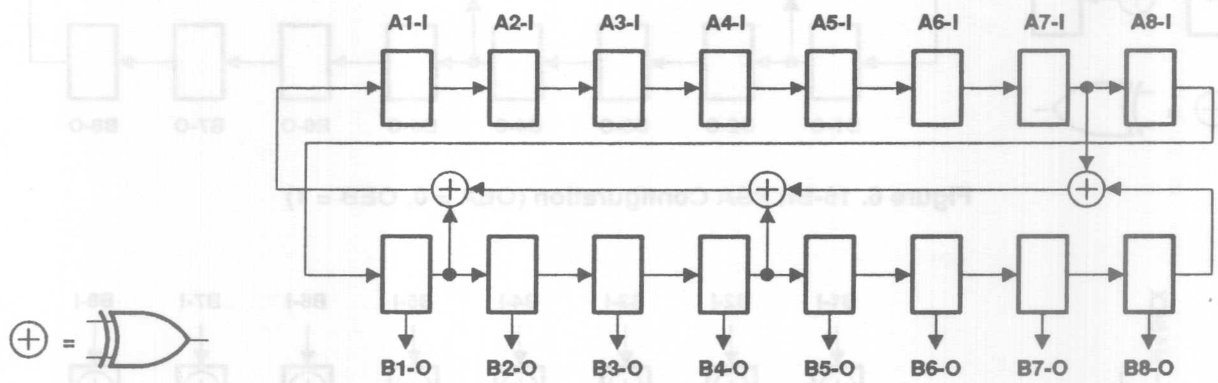


Figure 4. 16-Bit PRPG Configuration (OEA = 0, OEB = 1)

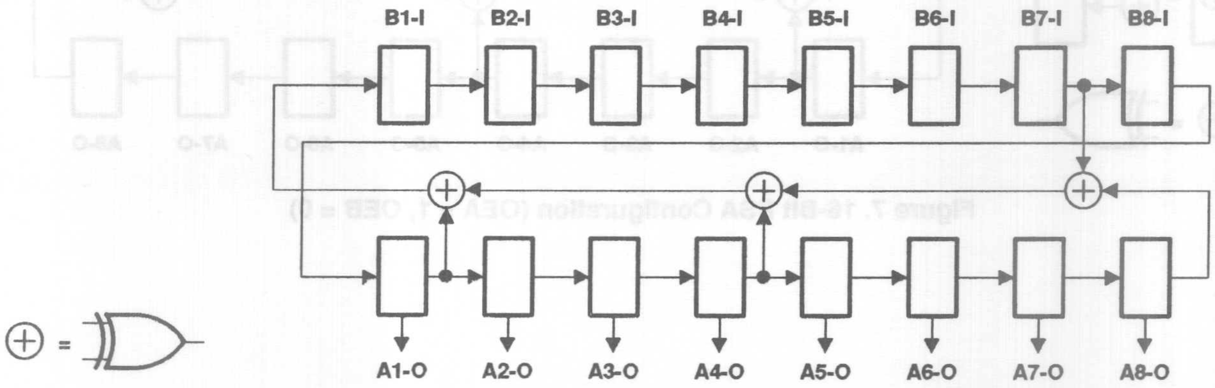


Figure 5. 16-Bit PRPG Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 illustrate the 16-bit linear-feedback shift register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

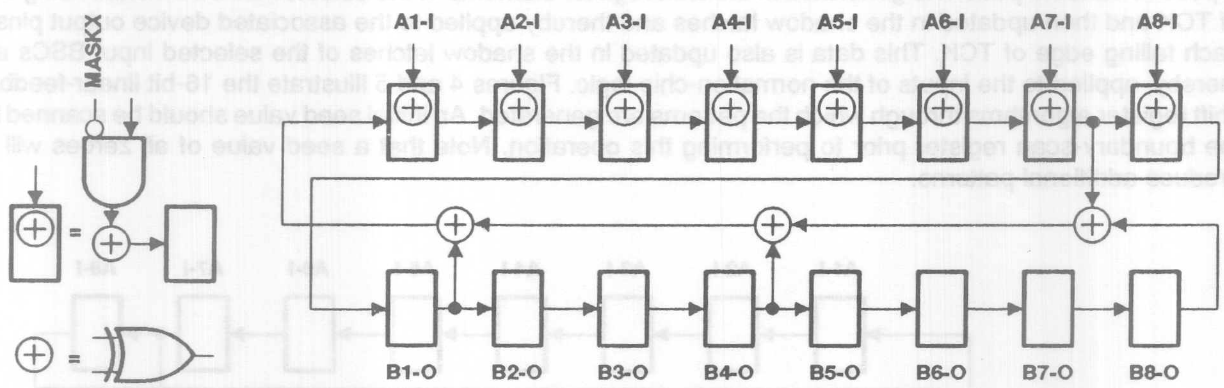


Figure 6. 16-Bit PSA Configuration (OEA = 0, OEB = 1)

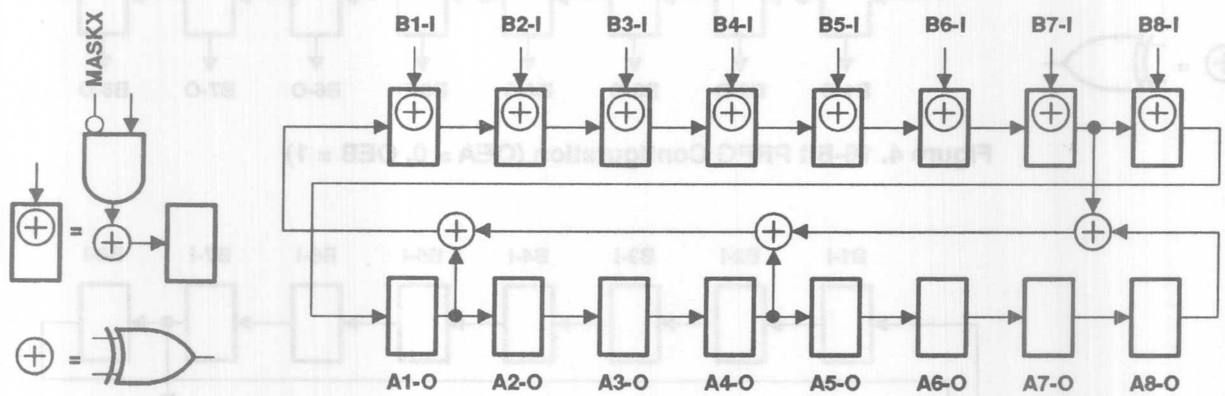


Figure 7. 16-Bit PSA Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 illustrate the 8-bit linear-feedback shift register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

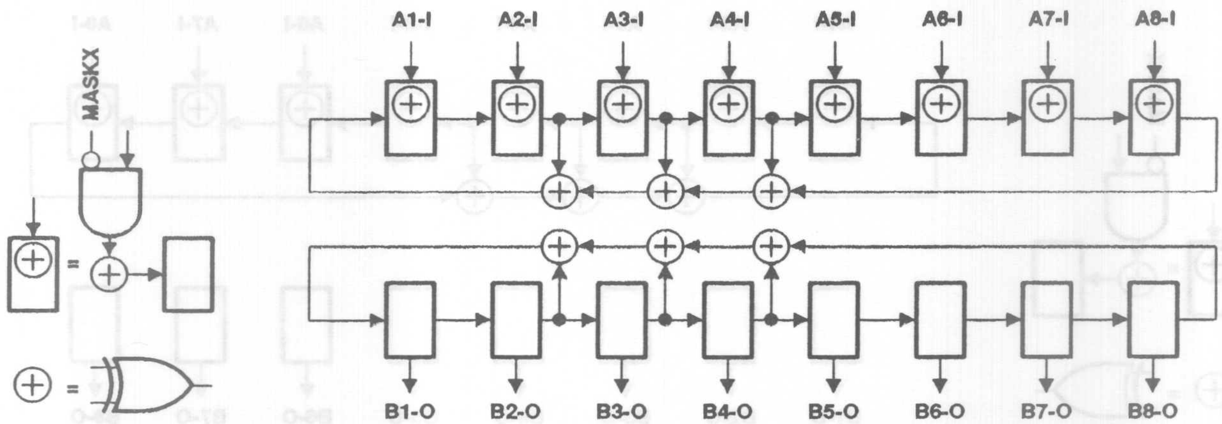


Figure 8. 8-Bit PSA/PRPG Configuration (OEA = 0, OEB = 1)

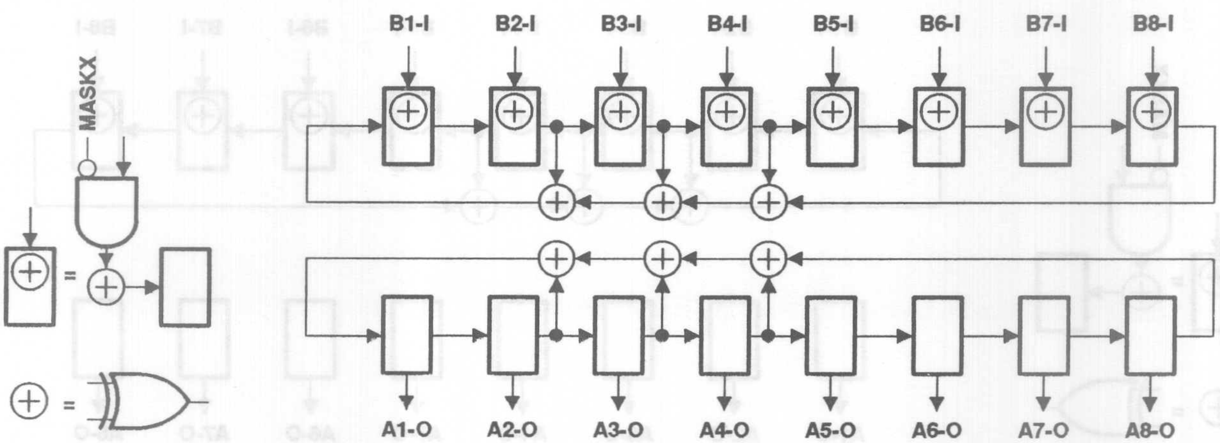


Figure 9. 8-Bit PSA/PRPG Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. In addition, the shift register elements of the opposite output BSCs are used to count carries out of the selected output BSCs and, thereby, extend the count to 16 bits. Figures 10 and 11 illustrate the 8-bit linear-feedback shift register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

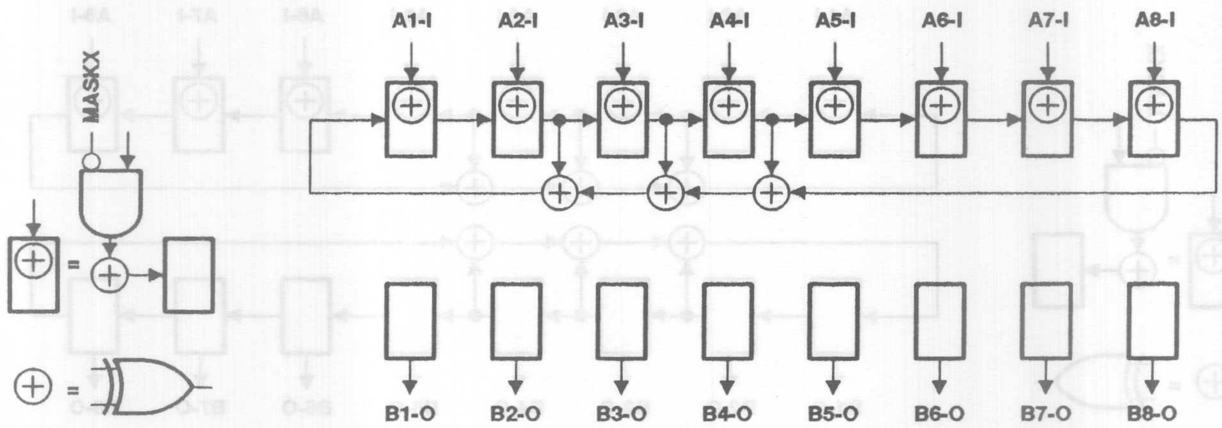


Figure 10. 8-Bit PSA/COUNT Configuration (OEA = 0, OEB = 1)

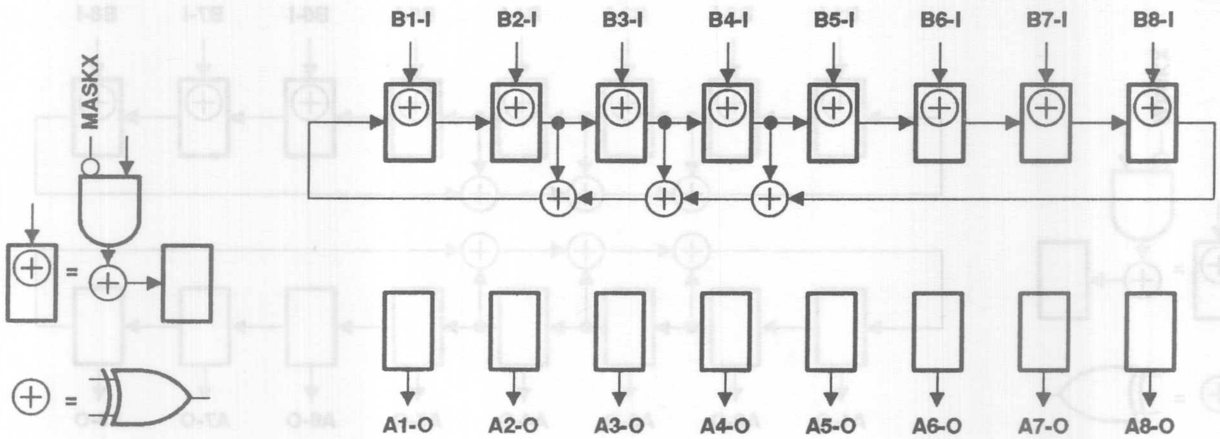


Figure 11. 8-Bit PSA/COUNT Configuration (OEA = 1, OEB = 0)

timing description

All test operations of the 'ABT8245 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in NO TAG) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 1. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active, and TDI is made valid, on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active, and TDI is made valid, on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

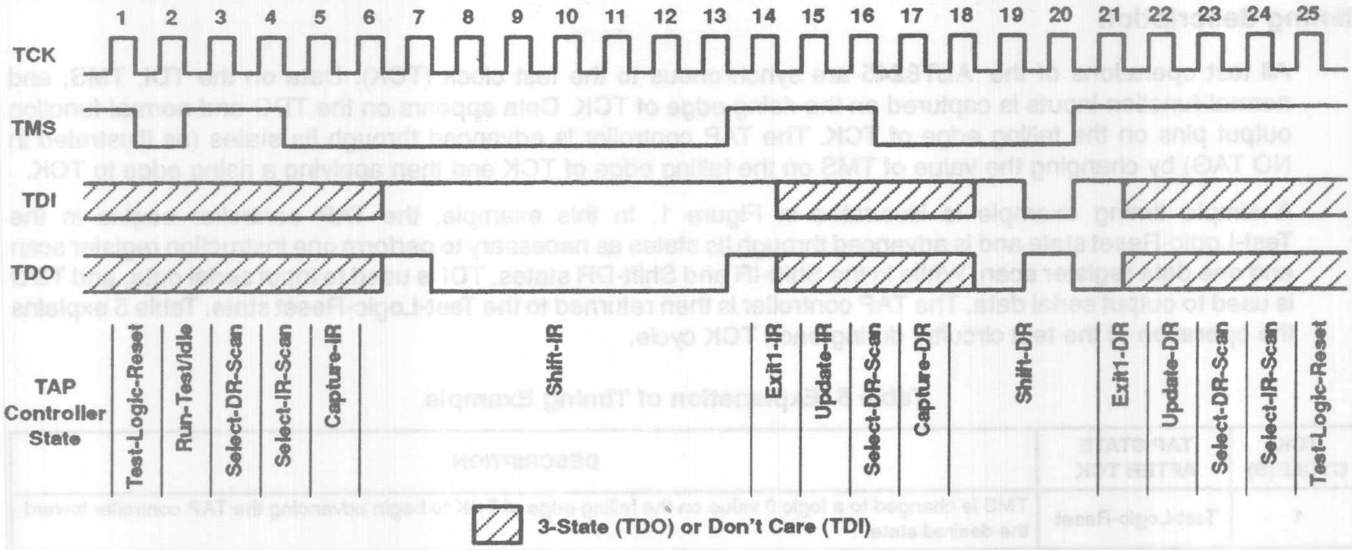


Figure 12. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1)	–0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8245	96 mA
SN74ABT8245	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8245 MIN	SN54ABT8245 MAX	SN74ABT8245 MIN	SN74ABT8245 MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			$T_A = 25°C$			SN54ABT8245		SN74ABT8245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		DIR, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0,	V_I or $V_O \le 5.5$ V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

			SN54ABT8245		SN74ABT8245		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A or B or DIR or $\overline{OE}$ before TCK↑	5		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A or B or DIR or $\overline{OE}$ after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

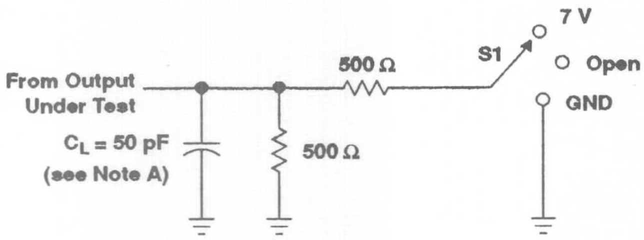
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C MIN	TYP	MAX	SN54ABT8245 MIN	MAX	SN74ABT8245 MIN	MAX	UNIT
t_{PLH}	A or B	B or A	2	3.5	4.3	2	5.1	2	4.8	ns
t_{PHL}			2	3.4	4.2	2	5.5	2	5.1	
t_{PZH}	$\overline{OE}$	B or A	2.5	4.5	5.5	2.5	6.9	2.5	6.8	ns
t_{PZL}			3	5.2	6	3	7.6	3	7.5	
t_{PHZ}	$\overline{OE}$	B or A	3	6.1	7.1	3	8.7	3	8.4	ns
t_{PLZ}			3	5.5	6.6	3	8	3	7.5	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

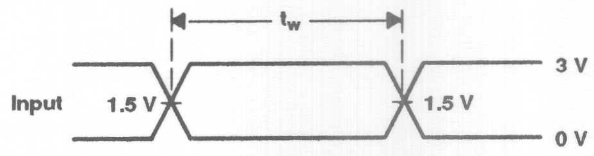
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C MIN	TYP	MAX	SN54ABT8245 MIN	MAX	SN74ABT8245 MIN	MAX	UNIT
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

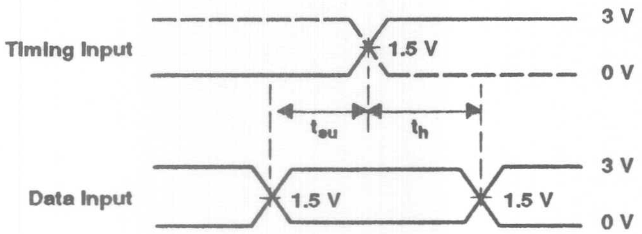


LOAD CIRCUIT FOR OUTPUTS

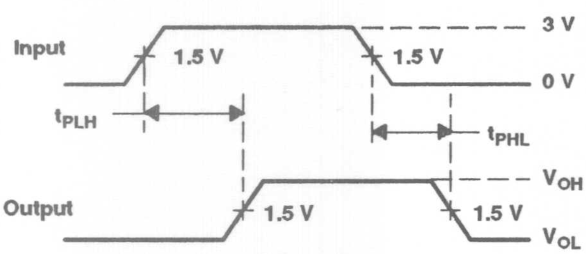
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



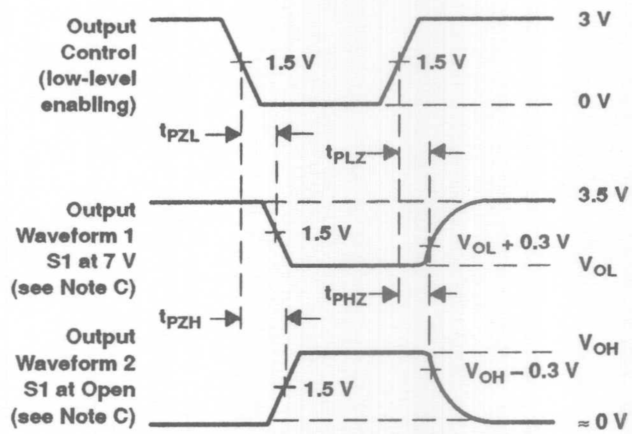
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



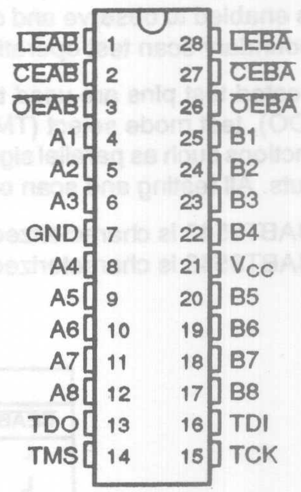
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

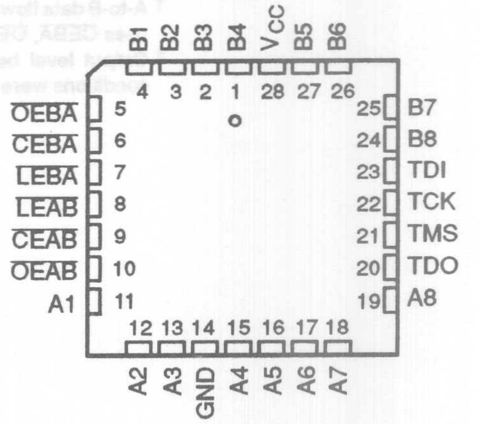
Figure 13. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74F543 and SN54/74ABT543 in the Normal Function Mode**
- ***SCOPE* ™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*Ⅱ*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8543 . . . JT PACKAGE
SN74ABT8543 . . . DL OR DW PACKAGE
(TOP VIEW)



SN54ABT8543 . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT8543 and SN74ABT8543 scan test devices with octal registered bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F543 and SN54/74ABT543 octal registered bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal registered bus transceivers.

Data flow in each direction is controlled by latch-enable ($\overline{\text{LEAB}}$ and $\overline{\text{LEBA}}$), chip-enable ($\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$), and output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when $\overline{\text{LEAB}}$ and $\overline{\text{CEAB}}$ are both low. When either $\overline{\text{LEAB}}$ or $\overline{\text{CEAB}}$ is high, the A data is latched. The B outputs are active when $\overline{\text{OEAB}}$ and $\overline{\text{CEAB}}$ are both low. When either $\overline{\text{OEAB}}$ or $\overline{\text{CEAB}}$ is high, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B but uses $\overline{\text{LEBA}}$, $\overline{\text{CEBA}}$, and $\overline{\text{OEBA}}$.

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description (continued)

In the test mode, the normal operation of the SCOPE™ registered bus transceiver is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

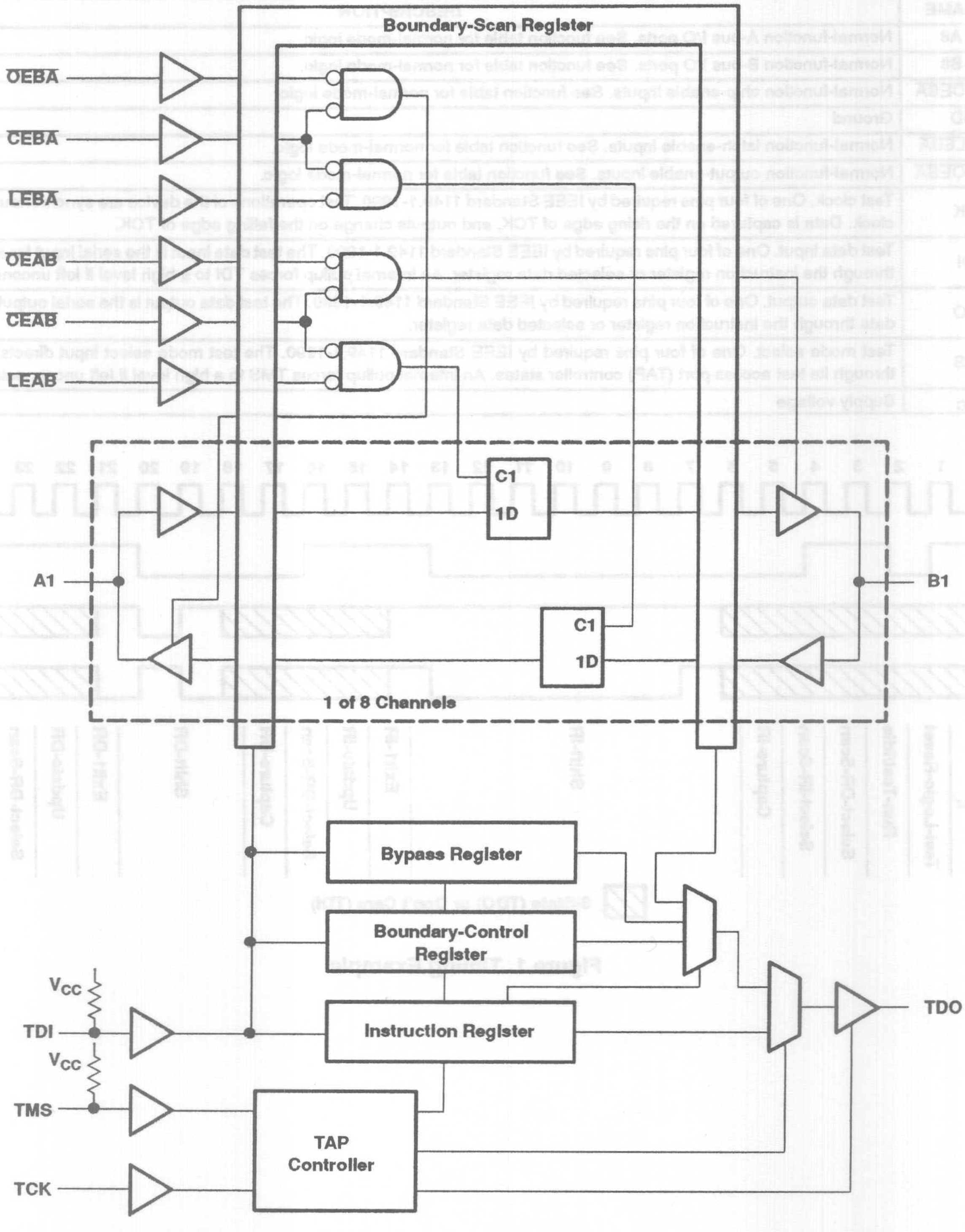
The SN54ABT8543 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74ABT8543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

INPUTS				OUTPUT
$\overline{\text{CEAB}}$	$\overline{\text{OEAB}}$	$\overline{\text{LEAB}}$	A	B
L	L	L	L	L
L	L	L	H	H
L	L	H	X	B_0‡
L	H	X	X	Z
H	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{CEBA}}$, $\overline{\text{OEBA}}$, and $\overline{\text{LEBA}}$.
‡ Output level before the indicated steady-state input conditions were established.

functional block diagram



Terminal Functions

PIN NAME	DESCRIPTION
A1 – A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1 – B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
$\overline{CEAB}$, $\overline{CEBA}$	Normal-function chip-enable inputs. See function table for normal-mode logic.
GND	Ground
$\overline{LEAB}$, $\overline{LEBA}$	Normal-function latch-enable inputs. See function table for normal-mode logic.
$\overline{OEAB}$, $\overline{OEBA}$	Normal-function output-enable inputs. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

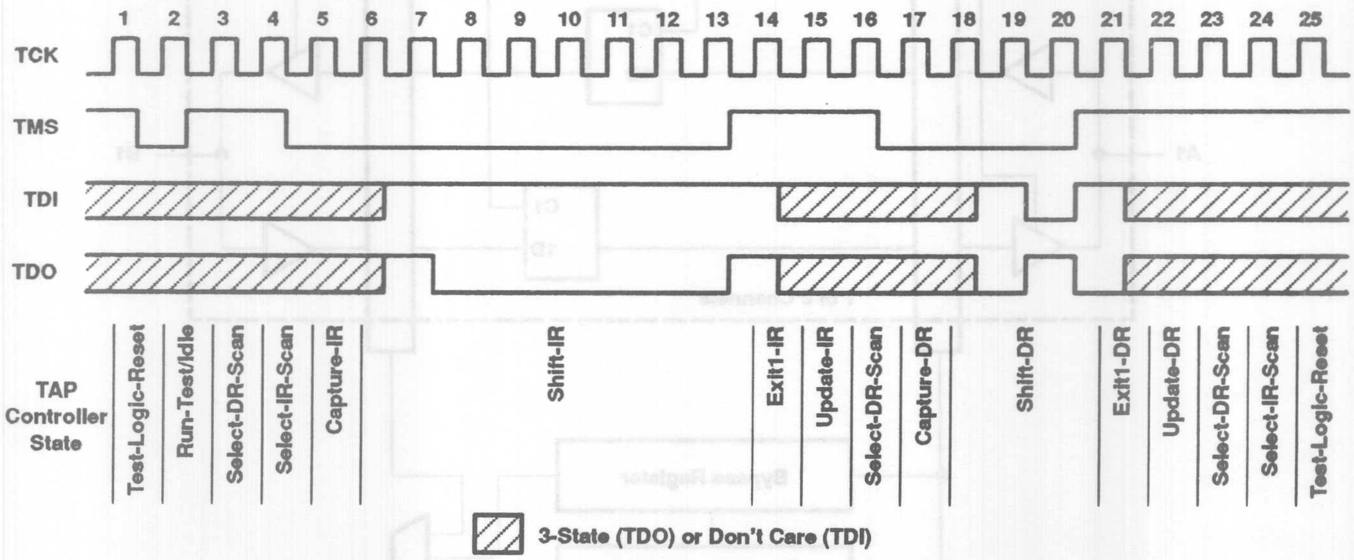


Figure 1. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8543 .... 96 mA
SN74ABT8543 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8543		SN74ABT8543		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	TYP†	MAX	SN54ABT8543 MIN	MAX	SN74ABT8543 MIN	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, $V_I = V_{CC}$ or GND		$\overline{CE}$, $\overline{LE}$, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	$V_I = V_{CC}$	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0,	V_I or $V_O \le$ 5.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, $V_I = V_{CC}$ or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_I	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 2)

			SN54ABT8543		SN74ABT8543		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	LEAB or LEBA high or low	3		3		ns
t_{su}	Setup time	A before $\overline{\text{LEAB}}$↑ or B before $\overline{\text{LEBA}}$↑	3		3		ns
t_h	Hold time	A after $\overline{\text{LEAB}}$↑ or B after $\overline{\text{LEBA}}$↑	0.5		0.5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 2)

			SN54ABT8543		SN74ABT8543		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A or B or $\overline{\text{CE}}$ or $\overline{\text{LE}}$ or $\overline{\text{OE}}$ before TCK↑	5		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A or B or $\overline{\text{CE}}$ or $\overline{\text{LE}}$ or $\overline{\text{OE}}$ after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 2)

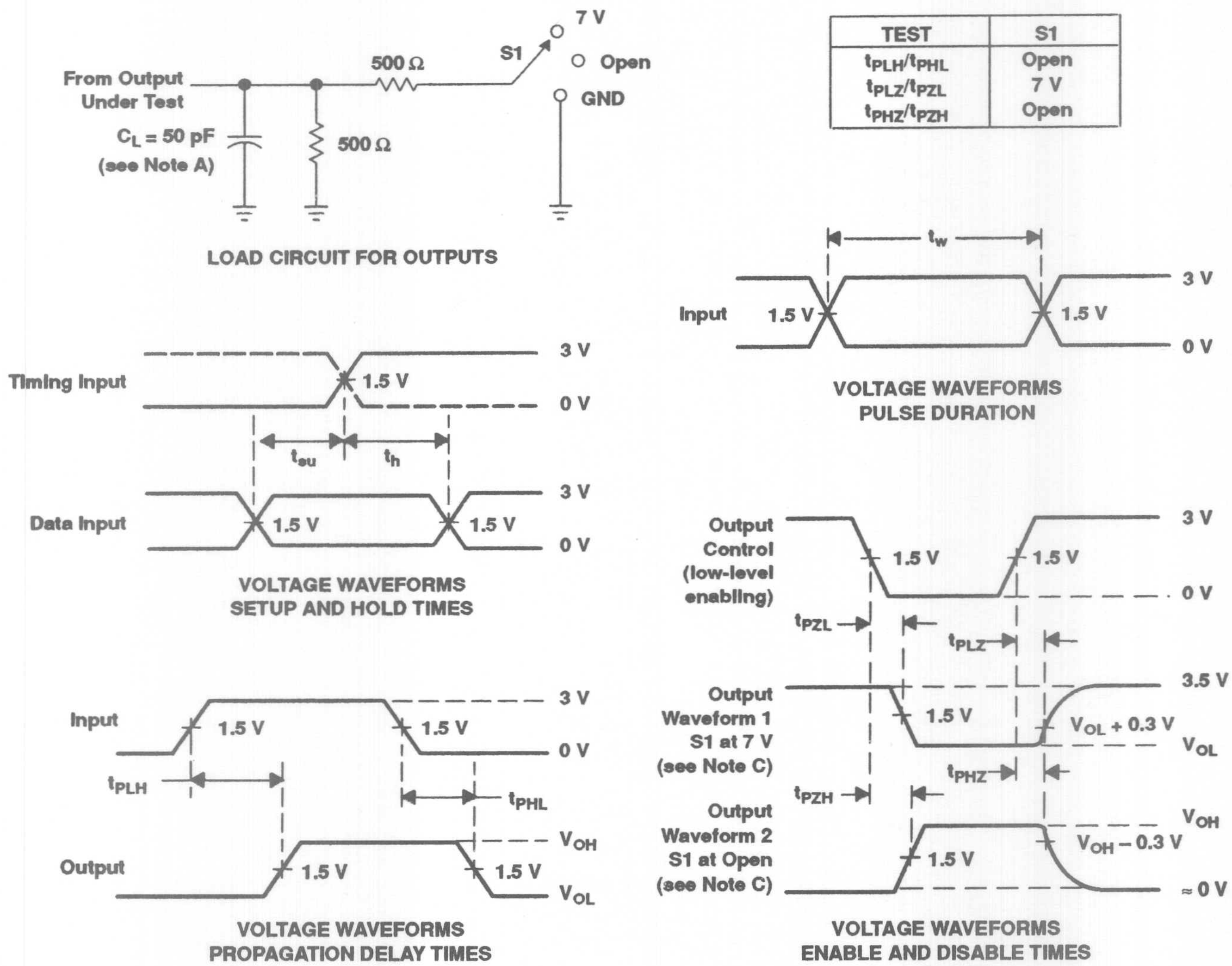
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8543		SN74ABT8543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ns
t_{PHL}			1.5	3.5	4.4	1.5	5.8	1.5	5.5	
t_{PLH}	$\overline{LEAB}$ or $\overline{LEBA}$	B or A	2	4.7	5.6	2	8.1	2	7.8	ns
t_{PHL}			1.5	4.1	5	1.5	7.3	1.5	6.9	
t_{PZH}	$\overline{CEAB}$ or $\overline{CEBA}$	B or A	2	4.2	5.2	2	7.5	2	7.2	ns
t_{PZL}			2	4.7	5.7	2	8.4	2	8.3	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.4	5.4	2	6.7	2	6.5	ns
t_{PZL}			2	5.2	6.2	2	7.6	2	7.5	
t_{PHZ}	$\overline{CEAB}$ or $\overline{CEBA}$	B or A	2.5	5.8	6.8	2.5	9.1	2.5	8.8	ns
t_{PLZ}			2.5	5.3	6.3	2.5	8.7	2.5	8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	5.9	6.9	2	8.3	2	7.9	ns
t_{PLZ}			2	5.2	6.2	2	7.8	2	7.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8543		SN74ABT8543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

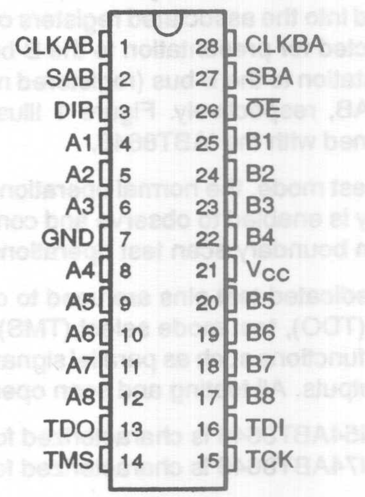


NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

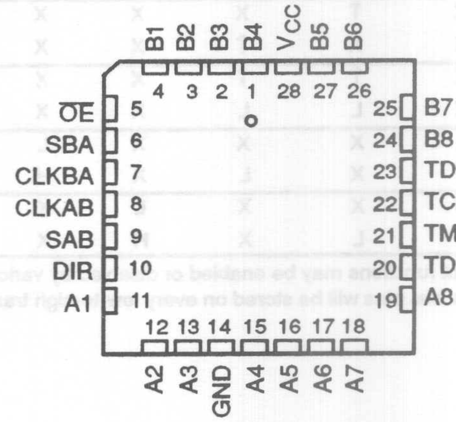
Figure 2. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74F646 and SN54/74ABT646 in the Normal Function Mode**
- ***SCOPE*™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPICIIB*™ BICMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8646 . . . JT PACKAGE
SN74ABT8646 . . . DL OR DW PACKAGE
(TOP VIEW)



SN54ABT8646 . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT8646 and SN74ABT8646 scan test devices with octal bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F646 and SN54/74ABT646 octal bus transceivers and registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers and registers.

Transceiver function is controlled by output-enable ($\overline{\text{OE}}$) and direction (DIR) inputs. When $\overline{\text{OE}}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{\text{OE}}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

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description (continued)

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that may be performed with the 'ABT8646.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

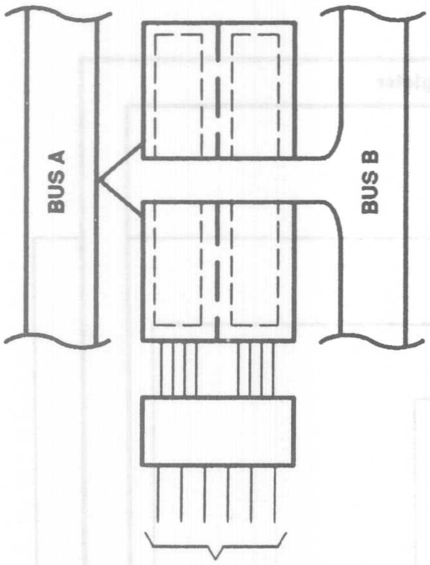
Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8646 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT8646 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

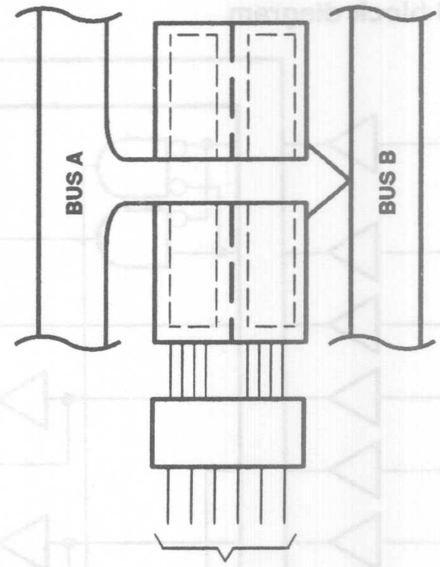
INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input disabled	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input disabled	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



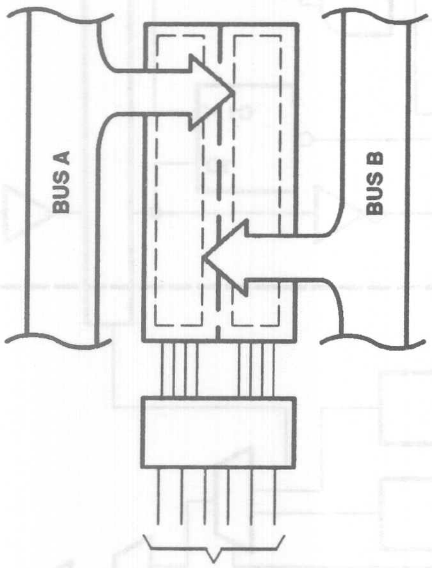
26 $\overline{OE}$	3 DIR	1 CLKAB	28 CLKBA	2 SAB	27 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



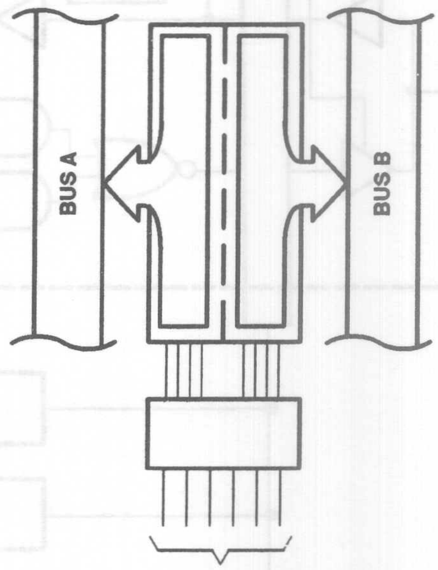
26 $\overline{OE}$	3 DIR	1 CLKAB	28 CLKBA	2 SAB	27 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



26 $\overline{OE}$	3 DIR	1 CLKAB	28 CLKBA	2 SAB	27 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



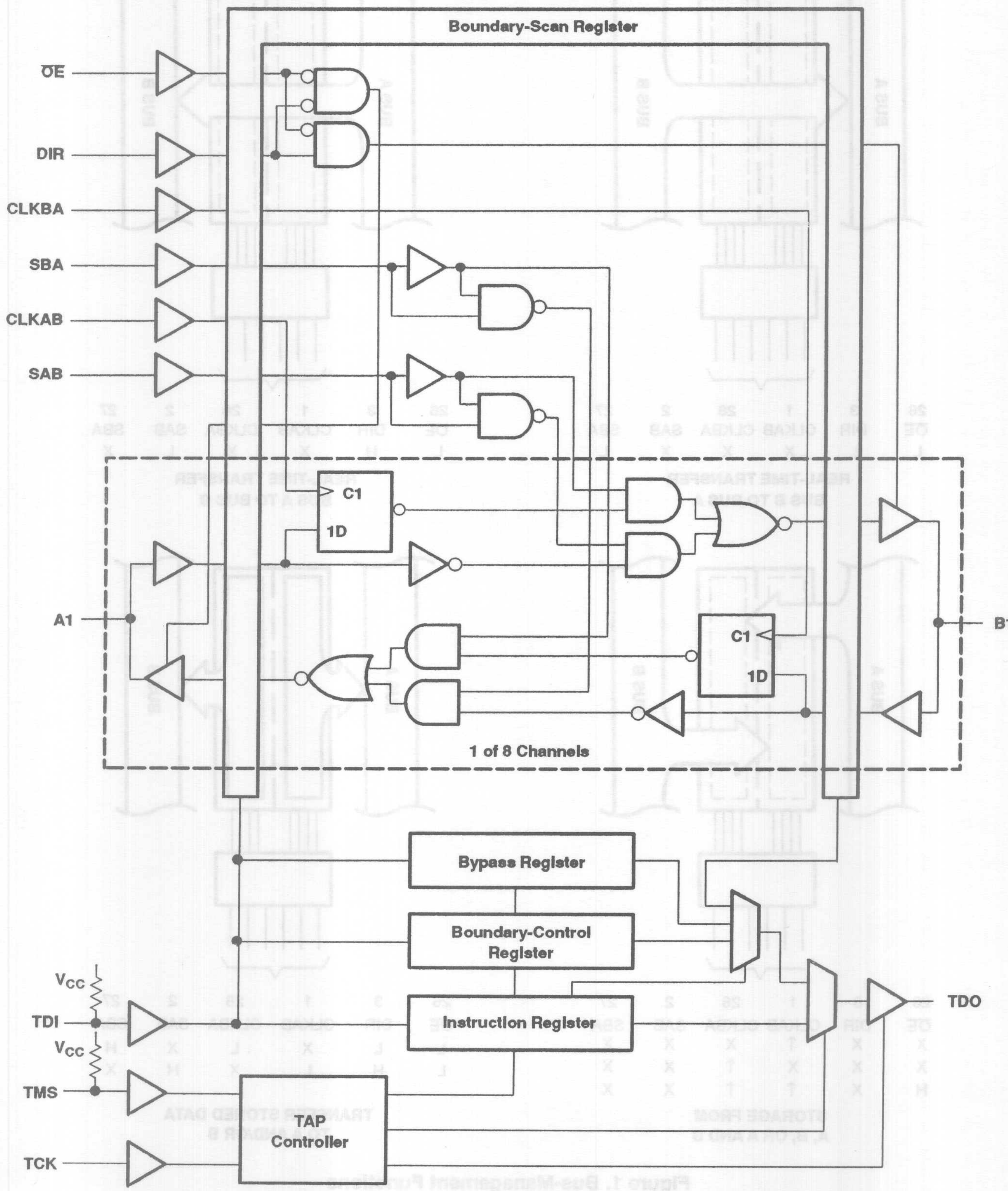
26 $\overline{OE}$	3 DIR	1 CLKAB	28 CLKBA	2 SAB	27 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus-Management Functions

Pin numbers shown are for DL, DW, and JT packages.

functional block diagram



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Terminal Functions

PIN NAME	DESCRIPTION
A1–A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
DIR	Normal-function direction-control input. See function table for normal-mode logic.
GND	Ground
$\overline{OE}$	Normal-function output-enable input. See function table for normal-mode logic.
SAB, SBA	Normal-function select inputs. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

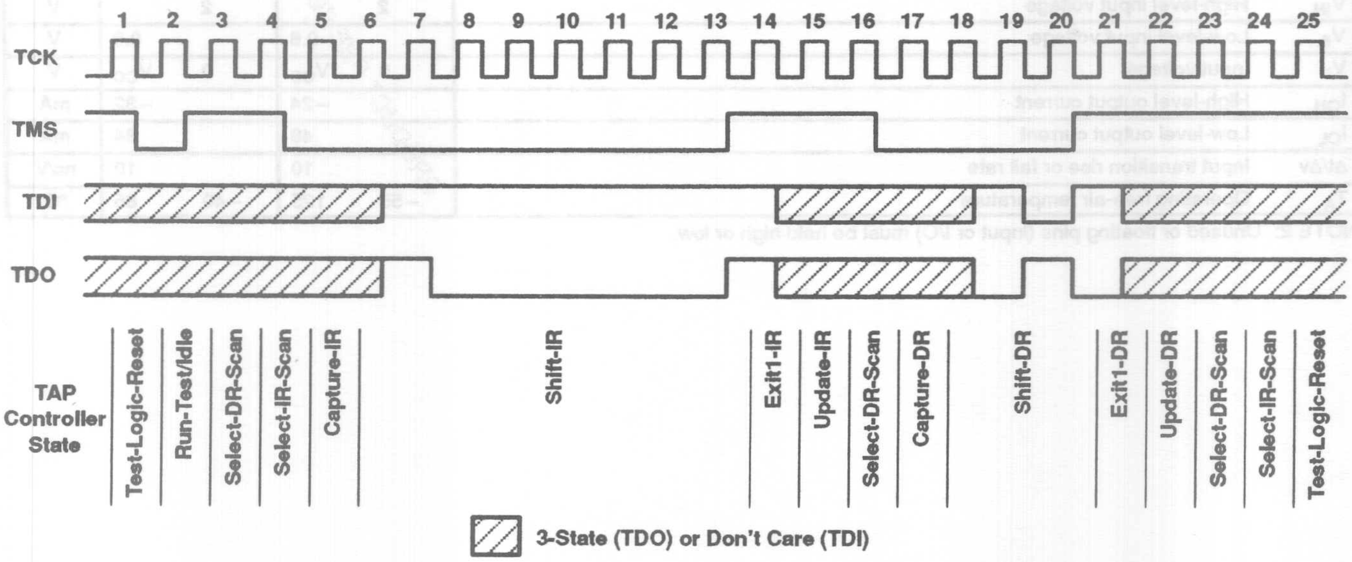


Figure 2. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8646 .... 96 mA
SN74ABT8646 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8646		SN74ABT8646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C TYP†	T_A = 25°C MAX	SN54ABT8646 MIN	SN54ABT8646 MAX	SN74ABT8646 MIN	SN74ABT8646 MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, DIR, $\overline{OE}$, S, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0,	V_I or V_O ≤ 5.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 3)

			SN54ABT8646		SN74ABT8646		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low	3		3		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	4.5		4.5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑	0		0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 3)

			SN54ABT8646		SN74ABT8646		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A, B, CLK, DIR, $\overline{OE}$, or S before TCK↑	5		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A, B, CLK, DIR, $\overline{OE}$, or S after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

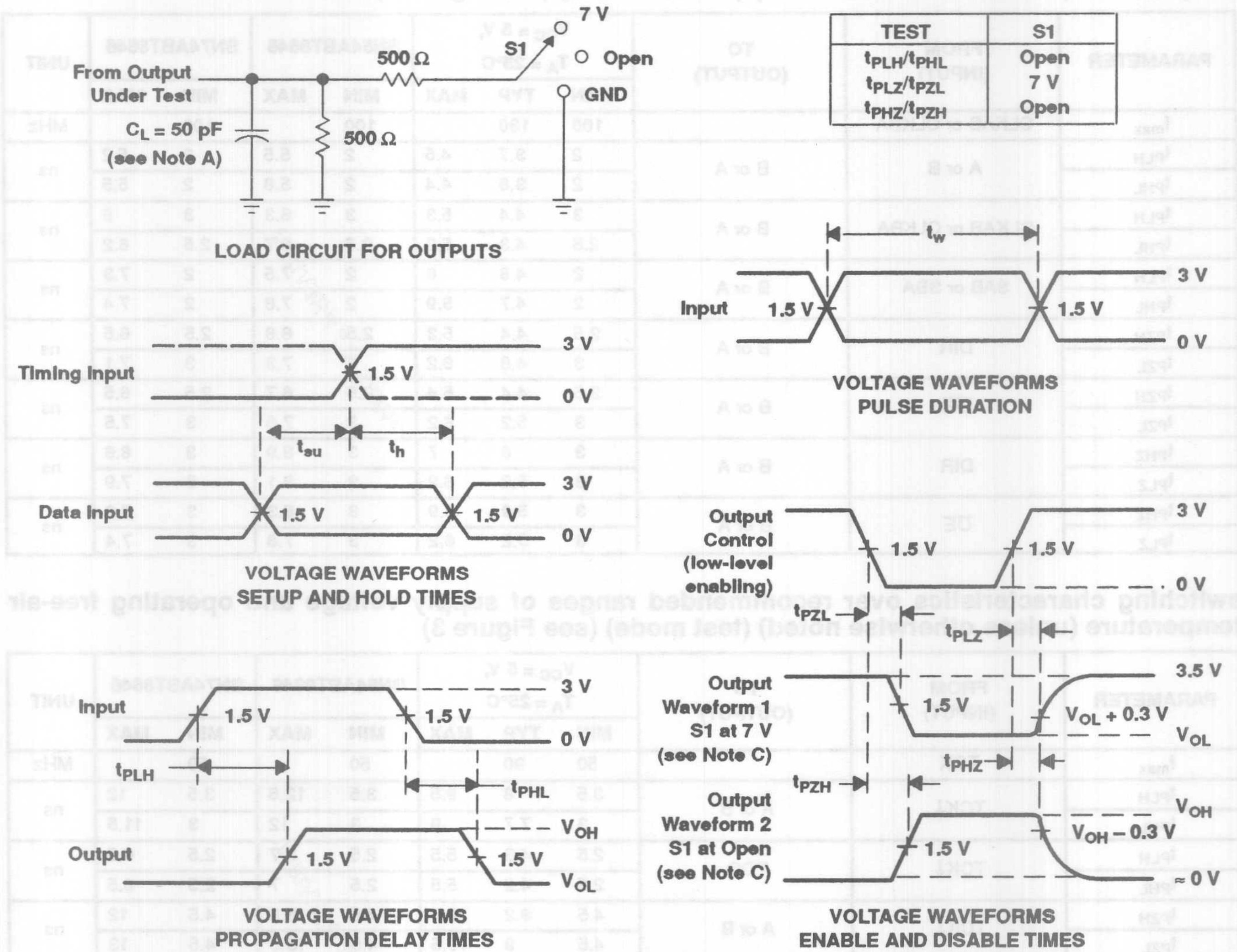
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8646		SN74ABT8646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ns
t_{PHL}			2	3.5	4.4	2	5.8	2	5,5	
t_{PLH}	CLKAB or CLKBA	B or A	3	4.4	5.3	3	6.3	3	6	ns
t_{PHL}			2.5	4.3	5.2	2.5	6.7	2.5	6.2	
t_{PLH}	SAB or SBA	B or A	2	4.8	6	2	7.5	2	7.3	ns
t_{PHL}			2	4.7	5.9	2	7.8	2	7.4	
t_{PZH}	DIR	B or A	2.5	4.4	5.3	2.5	6.6	2.5	6.5	ns
t_{PZL}			3	4.8	6.2	3	7.3	3	7.1	
t_{PZH}	$\overline{OE}$	B or A	2.5	4.4	5.4	2.5	6.7	2.5	6.5	ns
t_{PZL}			3	5.2	6.2	3	7.6	3	7.5	
t_{PHZ}	DIR	B or A	3	6	7	3	8.9	3	8.6	ns
t_{PLZ}			3	5.2	6.2	3	8.1	3	7.9	
t_{PHZ}	$\overline{OE}$	B or A	3	5.9	6.9	3	8.3	3	7.9	ns
t_{PLZ}			3	5.2	6.2	3	7.8	3	7.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8646		SN74ABT8646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION



NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

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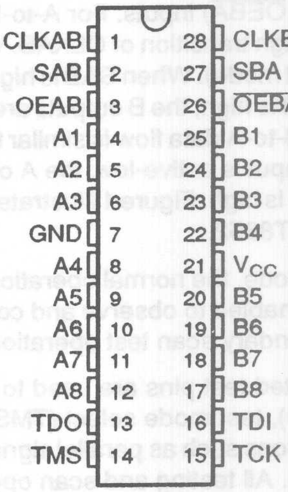
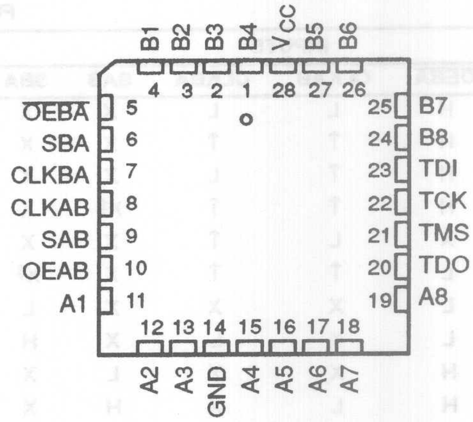
- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to SN54/74F652 and SN54/74ABT652 in the Normal Function Mode
- *SCOPE*™ Instruction Set:
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Even-Parity Opcodes
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art *EPIC*II*B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs

SN54ABT8652 . . . JT PACKAGE
SN74ABT8652 . . . DL OR DW PACKAGE
(TOP VIEW)



SN54ABT8652 . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT8652 and SN74ABT8652 scan test devices with octal bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F652 and SN54/74ABT652 octal bus transceivers and registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers and registers.

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description (continued)

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and $\overline{\text{OEBA}}$ inputs. Since the $\overline{\text{OEBA}}$ input is active-low, the A outputs are active when $\overline{\text{OEBA}}$ is low and are in the high-impedance state when OEBA is high. Figure 1 illustrates the four fundamental bus-management functions that may be performed with the 'ABT8652.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

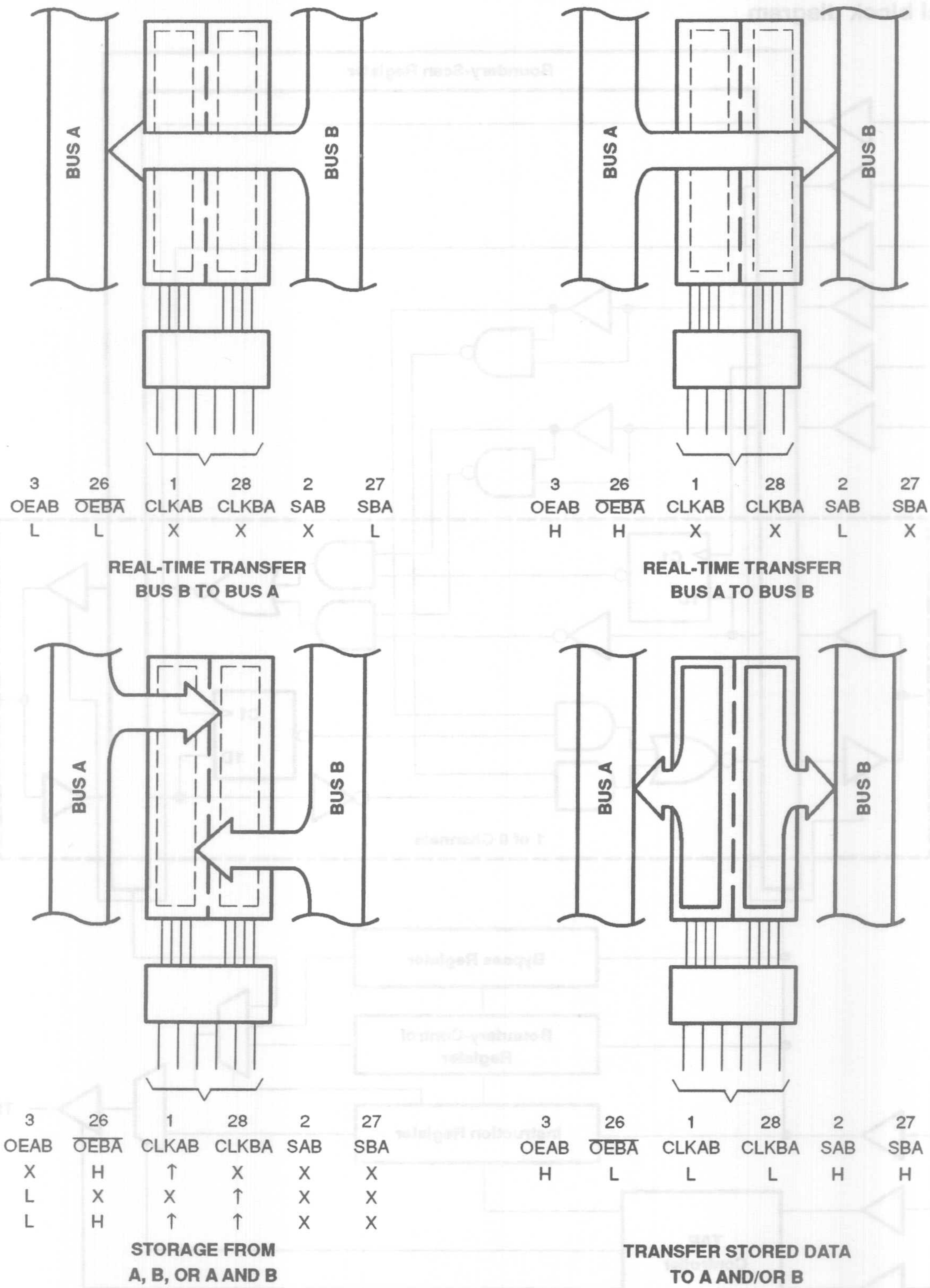
Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input disabled	Input disabled	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.



3	26	1	28	2	27
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A

3	26	1	28	2	27
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B

3	26	1	28	2	27
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A, B, OR A AND B

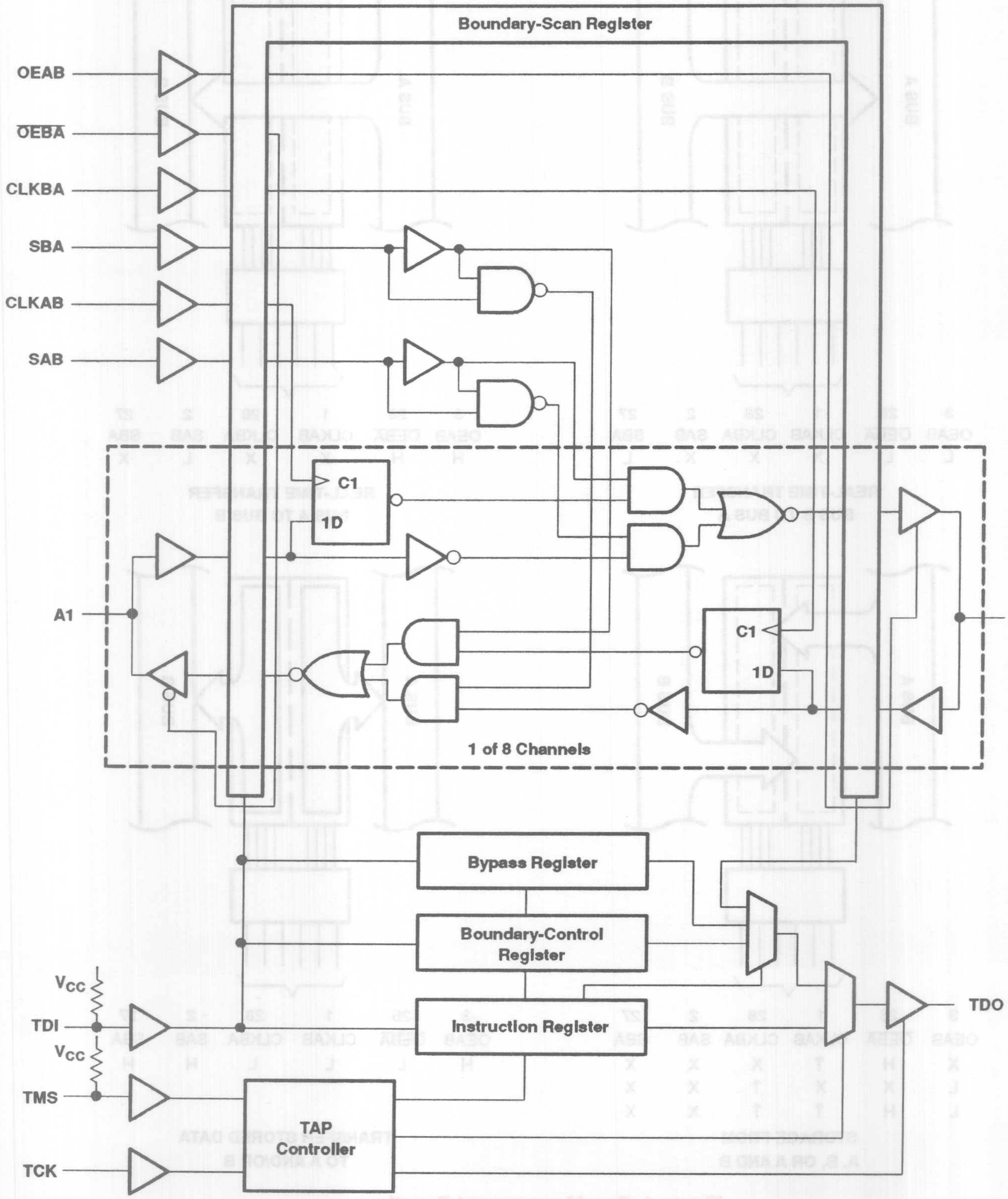
3	26	1	28	2	27
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus-Management Functions

Pin numbers shown are for DL, DW, and JT packages.

functional block diagram



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Terminal Functions

PIN NAME	DESCRIPTION
A1–A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
GND	Ground
OEAB, $\overline{OEBA}$	Normal-function output-enable inputs. See function table for normal-mode logic.
SAB, SBA	Normal-function select inputs. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

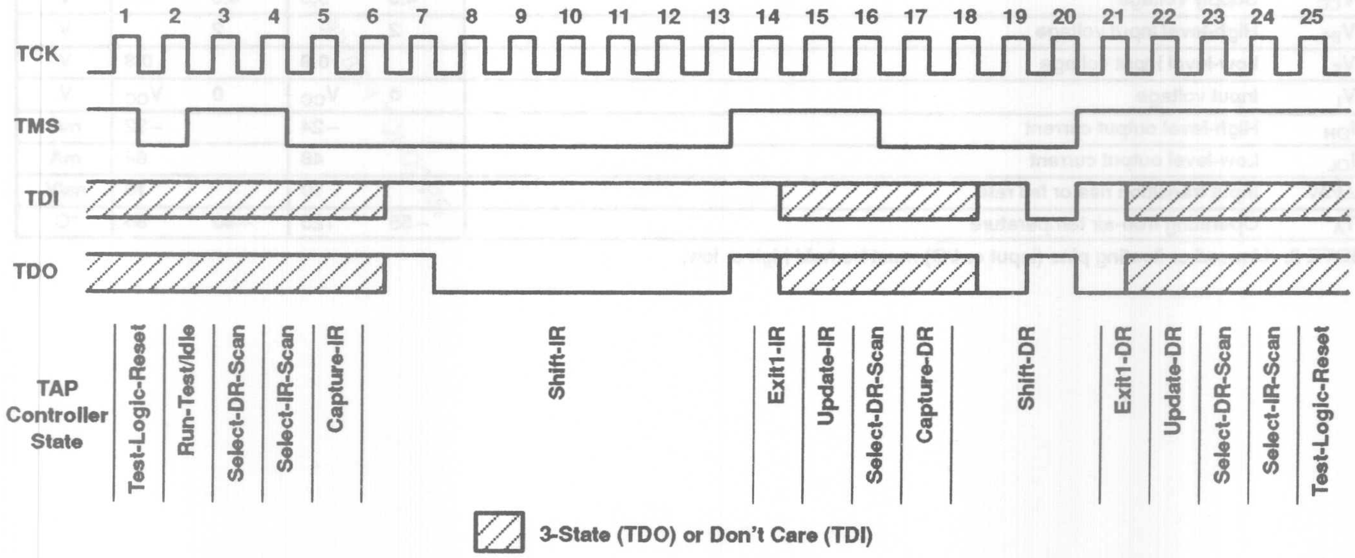


Figure 2. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8652 .... 96 mA
SN74ABT8652 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8652		SN74ABT8652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT8652		SN74ABT8652		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, OEAB, $\overline{OEBA}$, S, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0,	V_I or V_O ≤ 5.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 3)

			SN54ABT8652		SN74ABT8652		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low	3		3		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	4.5		4.5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑	0		0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 3)

			SN54ABT8652		SN74ABT8652		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A, B, CLK, OEAB, $\overline{OEBA}$, or S before TCK↑	5		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A, B, CLK, OEAB, $\overline{OEBA}$, or S after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

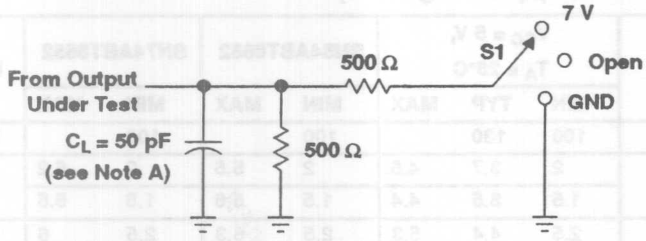
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8652		SN74ABT8652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ns
t_{PHL}			1.5	3.5	4.4	1.5	5.8	1.5	5.5	
t_{PLH}	CLKAB or CLKBA	B or A	2.5	4.4	5.3	2.5	6.3	2.5	6	ns
t_{PHL}			2.5	4.3	5.2	2.5	6.7	2.5	6.2	
t_{PLH}	SAB or SBA	B or A	2	4.8	6	2	7.5	2	7.3	ns
t_{PHL}			2	4.7	5.9	2	7.8	2	7.4	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A	2	4.4	5.4	2	6.7	2	6.5	ns
t_{PZL}			2	5.2	6.2	2	7.6	2	7.5	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A	2	5.9	6.9	2	8.3	2	7.9	ns
t_{PLZ}			2	5.2	6.2	2	7.8	2	7.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 3)

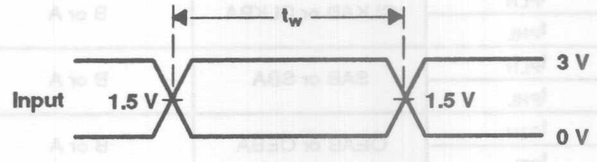
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8652		SN74ABT8652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

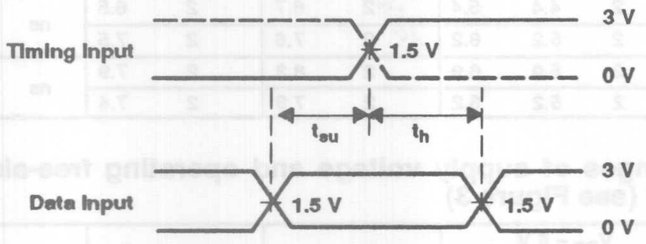


LOAD CIRCUIT FOR OUTPUTS

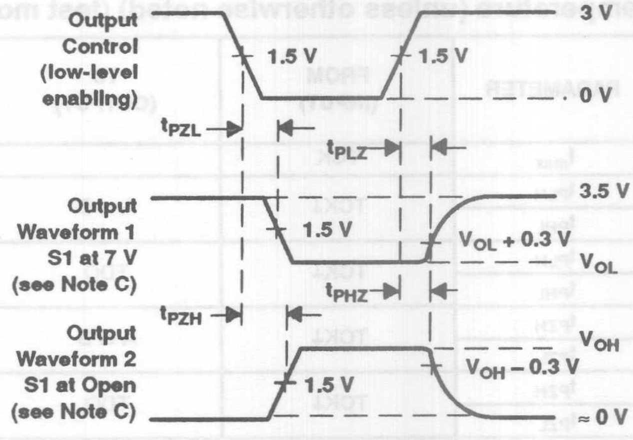
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

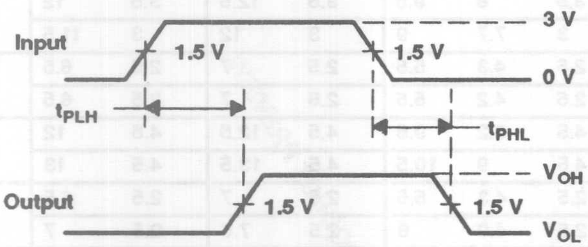


VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

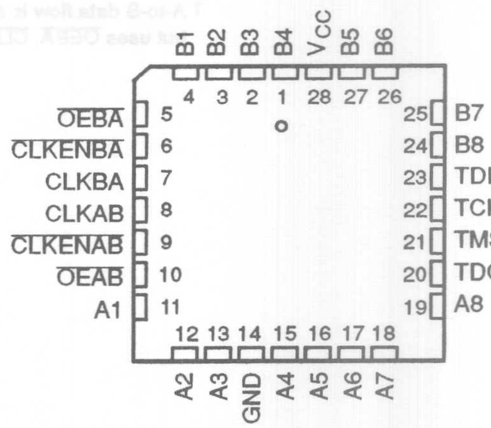
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE* ™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74BCT2952 and SN54/74ABT2952 in the Normal Function Mode**
- ***SCOPE* ™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*II*B*™ BICMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8952 . . . JT PACKAGE
SN74ABT8952 . . . DL OR DW PACKAGE
(TOP VIEW)

SN54ABT8952 . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT8952 and SN74ABT8952 scan test devices with octal registered bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74BCT2952 and SN54/74ABT2952 octal registered bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal registered bus transceivers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs. For A-to-B data flow, A-bus data is stored in the associated registers on the low-to-high transition of CLKAB provided that $\overline{CLKENAB}$ is low. Otherwise, if $\overline{CLKENAB}$ is high or CLKAB remains at a static low or high level, the register contents are not changed. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B but uses CLKBA, $\overline{CLKENBA}$, and $\overline{OEBA}$.

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description (continued)

In the test mode, the normal operation of the SCOPE™ registered bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

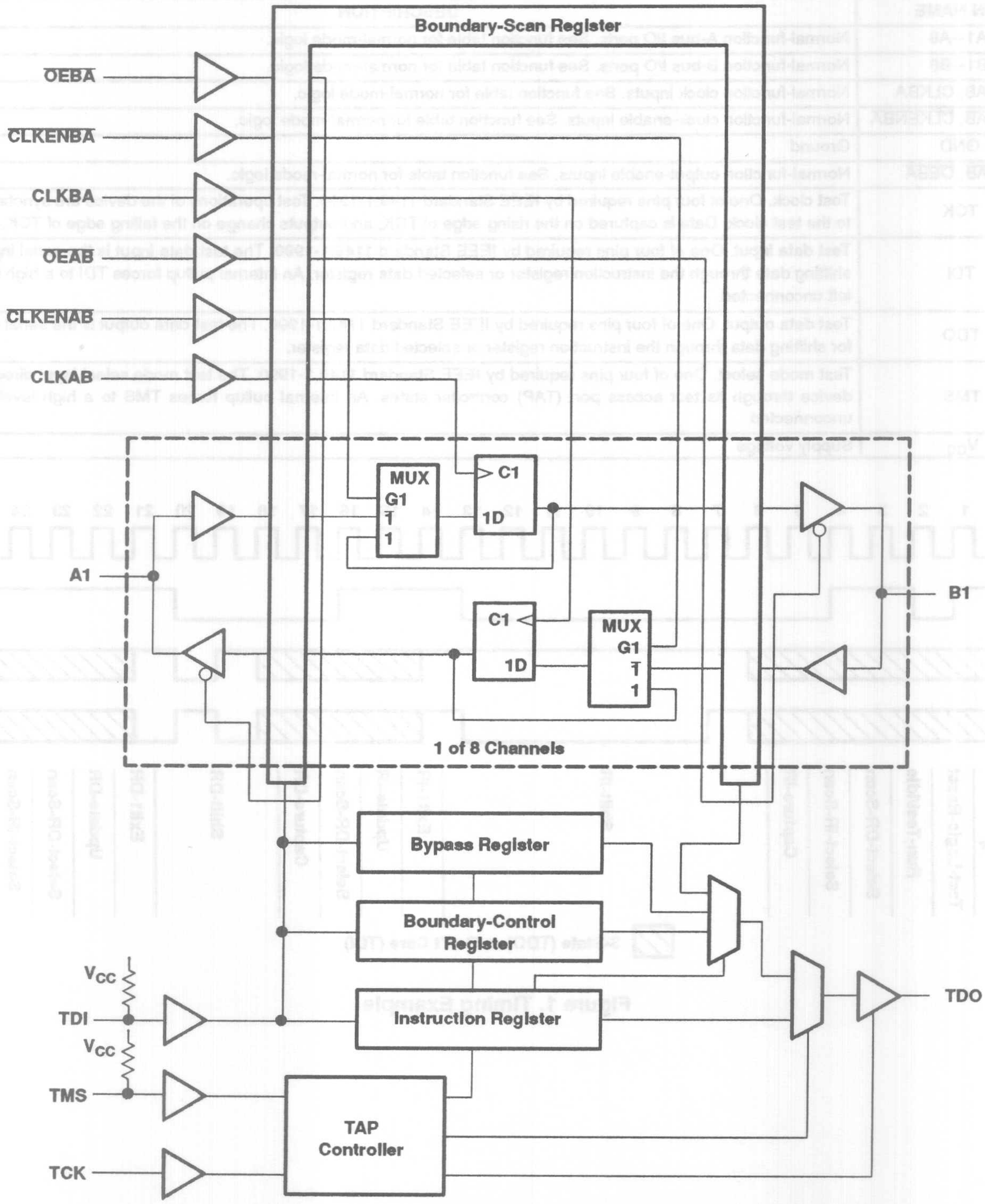
The SN54ABT8952 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT8952 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

INPUTS				OUTPUT
$\overline{\text{OEAB}}$	$\overline{\text{CLKENAB}}$	CLKAB	A	B
L	L	↑	L	L
L	L	↑	H	H
L	H	X	X	B_0
L	X	L	X	B_0
H	X	X	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, $\overline{\text{CLKENBA}}$, and CLKBA.

functional block diagram



Terminal Functions

PIN NAME	DESCRIPTION
A1–A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
$\overline{CLKENAB}$, $\overline{CLKENBA}$	Normal-function clock-enable inputs. See function table for normal-mode logic.
GND	Ground
$\overline{OEAB}$, $\overline{OEBA}$	Normal-function output-enable inputs. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

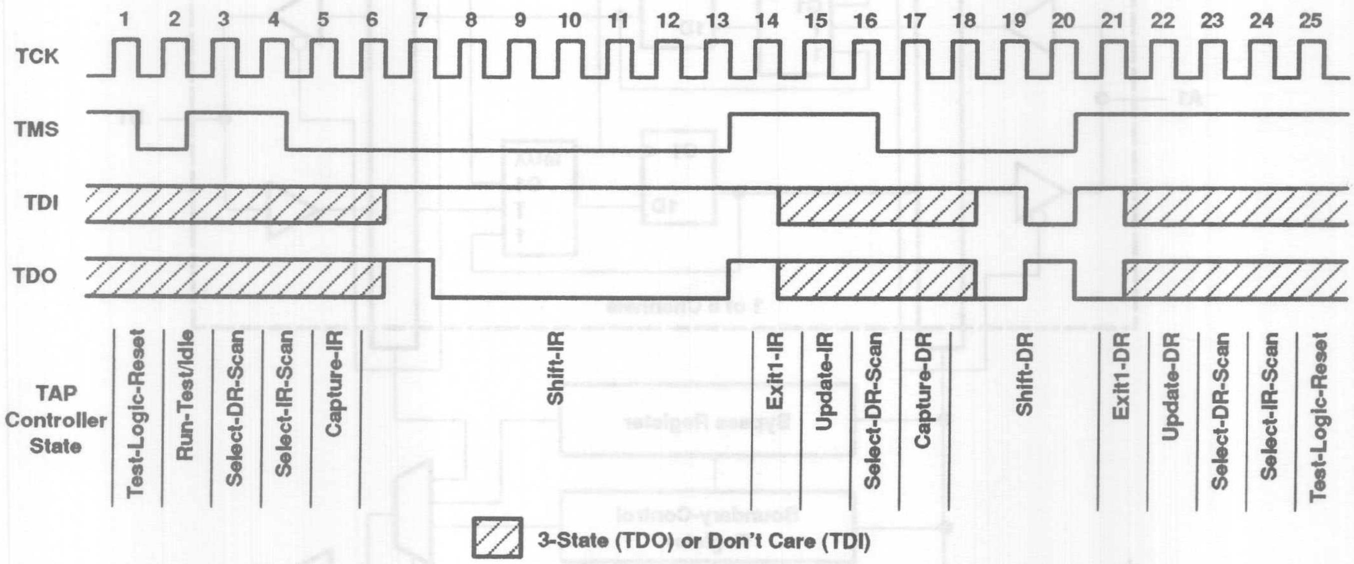


Figure 1. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8952 .... 96 mA
SN74ABT8952 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8952		SN74ABT8952		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C TYP†	T_A = 25°C MAX	SN54ABT8952 MIN	SN54ABT8952 MAX	SN74ABT8952 MIN	SN74ABT8952 MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, $\overline{CLKEN}$, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0,	V_I or $V_O \leq$ 5.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 2)

			SN54ABT8952		SN74ABT8952		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low	3		3		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	4.5		4.5		ns
		$\overline{\text{CLKEN}}$ before CLK↑	4.5		4.5		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑	0		0		ns
		$\overline{\text{CLKEN}}$ after CLK↑	0		0		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 2)

			SN54ABT8952		SN74ABT8952		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A, B, CLK, $\overline{\text{CLKEN}}$, or $\overline{\text{OE}}$ before TCK↑	5		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A, B, CLK, $\overline{\text{CLKEN}}$, or $\overline{\text{OE}}$ after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

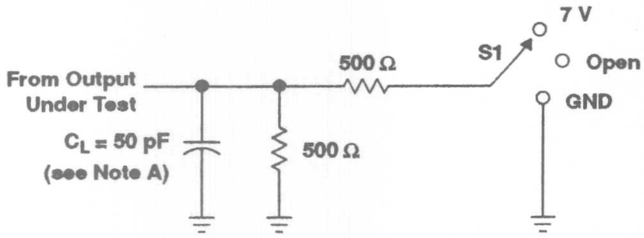
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8952		SN74ABT8952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLK	A or B	100	130		100		100		MHz
t_{PLH}	CLKAB or CLKBA	B or A	3	4.6	5.4	3	6.5	3	6.3	ns
t_{PHL}			2.5	3.8	4.6	2.5	5.5	2.5	5.3	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.1	4.9	2	5.9	2	5.8	ns
t_{PZL}			2.5	4.7	5.5	2.5	7.1	2.5	6.9	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2.5	5.3	6.1	2.5	7.5	2.5	7.3	ns
t_{PLZ}			3	4.5	5.3	3	6.3	3	6.1	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 2)

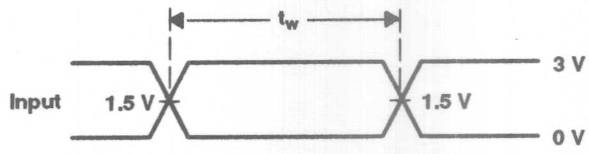
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8952		SN74ABT8952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

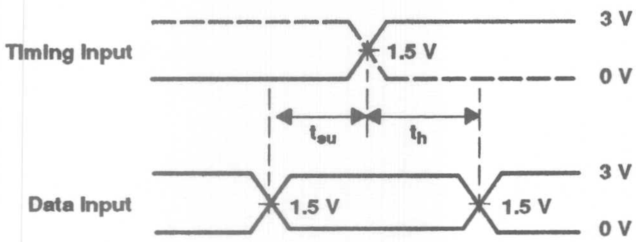


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

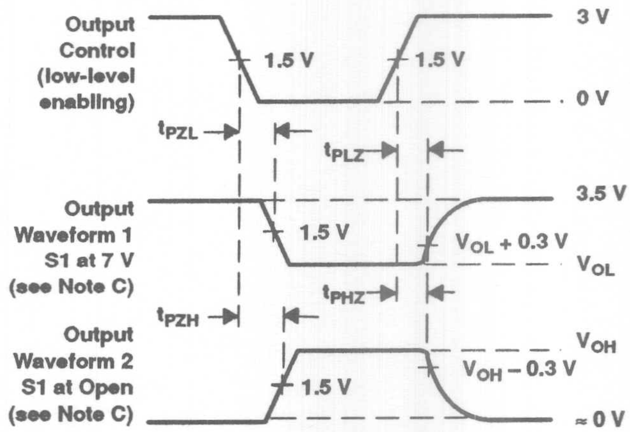
LOAD CIRCUIT FOR OUTPUTS



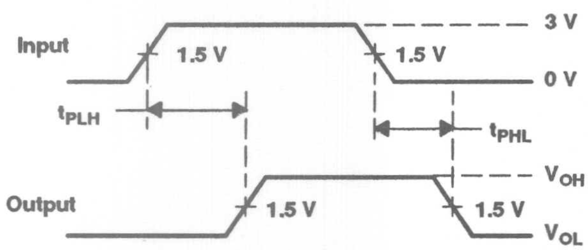
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- Members of the Texas Instruments *SCOPE* ™ Family of Testability Products
- Members of the Texas Instruments *Widebus* ™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE* ™ Instruction Set
  - IEEE Standard 1149.1-1990-Required Instructions and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- State-of-the-Art *EPIC-IIB* ™ BICMOS Design Significantly Reduces Power Dissipation
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

SN54ABT18245 . . . WD PACKAGE
SN74ABT18245 . . . DL PACKAGE
(TOP VIEW)

1DIR	1	56	1$\overline{OE}$
1B1	2	55	1A1
1B2	3	54	1A2
GND	4	53	GND
1B3	5	52	1A3
1B4	6	51	1A4
V_{CC}	7	50	V_{CC}
1B5	8	49	1A5
1B6	9	48	1A6
1B7	10	47	1A7
GND	11	46	GND
1B8	12	45	1A8
1B9	13	44	1A9
2B1	14	43	2A1
2B2	15	42	2A2
2B3	16	41	2A3
2B4	17	40	2A4
GND	18	39	GND
2B5	19	38	2A5
2B6	20	37	2A6
2B7	21	36	2A7
V_{CC}	22	35	V_{CC}
2B8	23	34	2A8
2B9	24	33	2A9
GND	25	32	GND
2DIR	26	31	2$\overline{OE}$
TDO	27	30	TDI
TMS	28	29	TCK

description

The SN54ABT18245 and SN74ABT18245 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

PRODUCT PREVIEW

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description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN74ABT18245 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

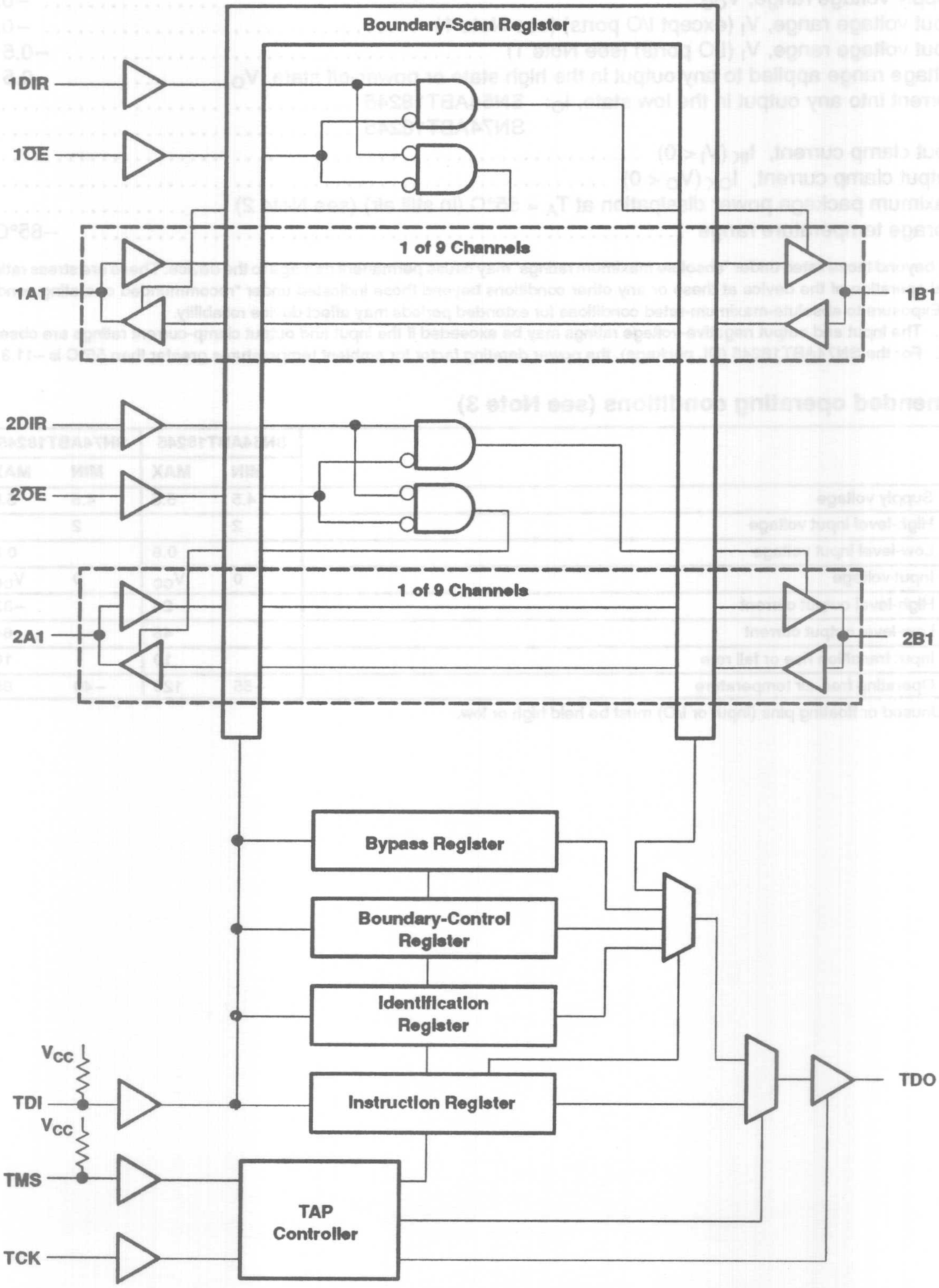
The SN54ABT18245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT18245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18245 .... 96 mA
SN74ABT18245 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2) .... 950 mW
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18245 (DL package), the power derating factor for ambient temperatures greater than 55°C is –11.3 mW/°C.

recommended operating conditions (see Note 3)

		SN54ABT18245		SN74ABT18245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS		T_A = 25°C MIN	T_A = 25°C TYP†	T_A = 25°C MAX	SN54ABT18245 MIN	SN54ABT18245 MAX	SN74ABT18245 MIN	SN74ABT18245 MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	DIR, $\overline{OE}$, TCK			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}‡	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V, V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0, V_I or V_O ≤ 5.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND, A or B ports	Outputs high			4		4		4	mA
		Outputs low			80		80		80	
		Outputs disabled			4		4		4	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V	TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

			SN54ABT18245 MIN	SN54ABT18245 MAX	SN74ABT18245 MIN	SN74ABT18245 MAX	UNIT
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			5		ns
t_{su}	Setup time	A, B, DIR or $\overline{OE}$ before TCK↑			5		ns
		TDI before TCK↑			6		
		TMS before TCK↑			6		
t_h	Hold time	A, B, DIR or $\overline{OE}$ after TCK↑			0		ns
		TDI after TCK↑			0		
		TMS after TCK↑			0		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 4: Preliminary specifications based on SPICE analysis

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18245		SN74ABT18245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A						1	6	ns
t_{PHL}								1	6	
t_{PZH}	$\overline{OE}$	B or A						2	7.5	ns
t_{PZL}								2	7.5	
t_{PHZ}	$\overline{OE}$	B or A						2	7.5	ns
t_{PLZ}								2	7.5	

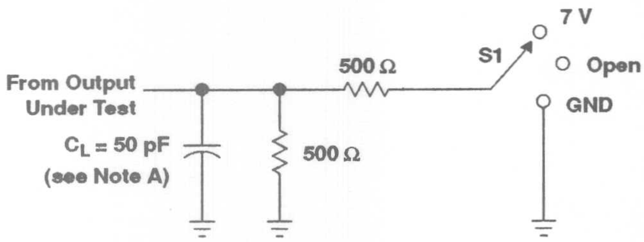
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18245		SN74ABT18245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						3	12	ns
t_{PHL}								3	12	
t_{PLH}	TCK↓	TDO						2	7	ns
t_{PHL}								2	7	
t_{PZH}	TCK↓	A or B						3	14	ns
t_{PZL}								3	14	
t_{PZH}	TCK↓	TDO						2	8	ns
t_{PZL}								2	8	
t_{PHZ}	TCK↓	A or B						3	14	ns
t_{PLZ}								3	14	
t_{PHZ}	TCK↓	TDO						2	8	ns
t_{PLZ}								2	8	

NOTE 4: Preliminary specifications based on SPICE analysis

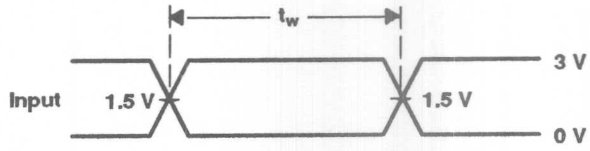
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

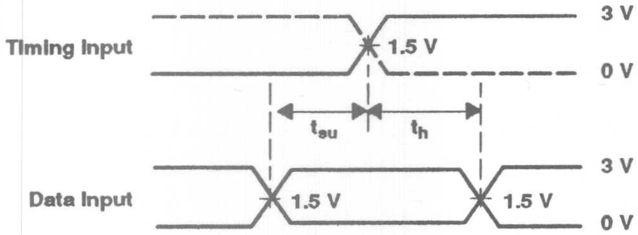


LOAD CIRCUIT FOR OUTPUTS

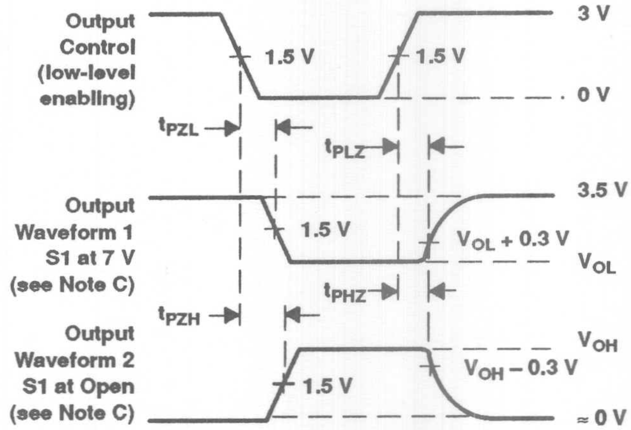
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



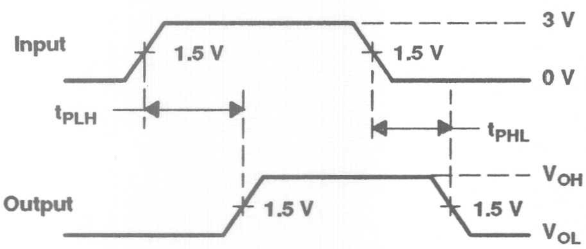
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

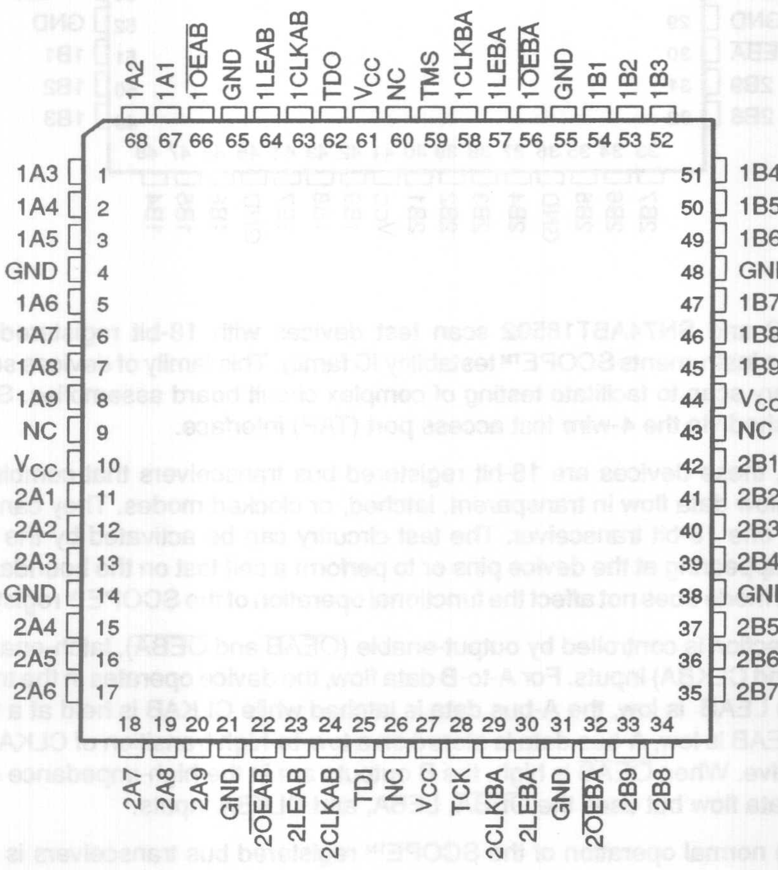
PRODUCT PREVIEW

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (W)**

SN54ABT18502 . . . W PACKAGE
(TOP VIEW)



NC – No internal connection

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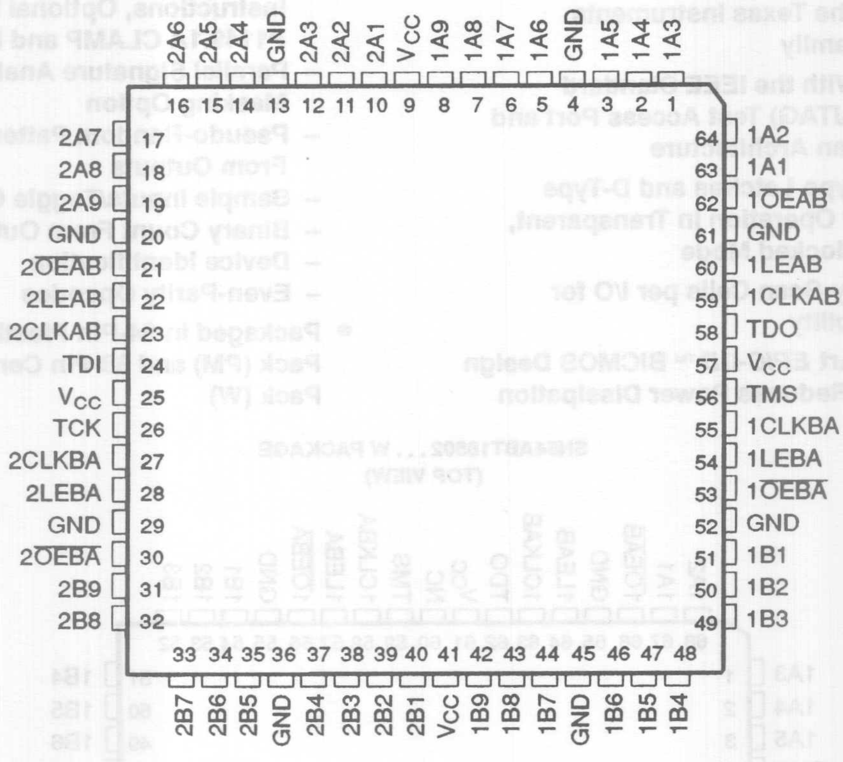
SN74ABT18502 . . . PM PACKAGE
(TOP VIEW)



description

The SN54ABT18502 and SN74ABT18502 scan test devices with 18-bit registered bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit registered bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ registered bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{\text{OEAB}}$ is low, the B outputs are active. When $\overline{\text{OEAB}}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{\text{OEBA}}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ registered bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18502 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT18502 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

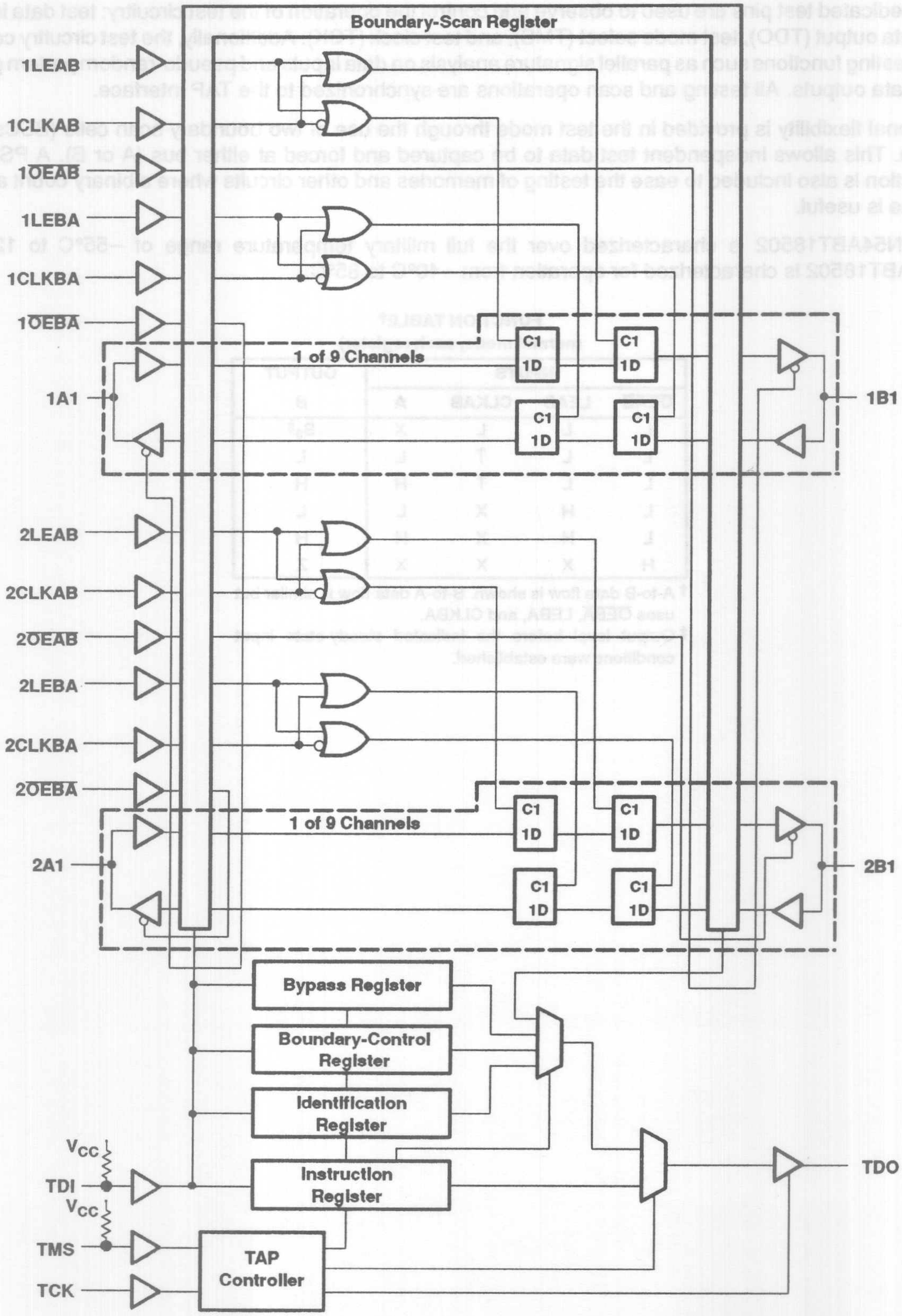
INPUTS				OUTPUT
$\overline{\text{OEAB}}$	LEAB	CLKAB	A	B
L	L	L	X	B_0‡
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18502 .... 96 mA
SN74ABT18502 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2) .... 885 mW
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18502 (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

recommended operating conditions (see Note 3)

		SN54ABT18502		SN74ABT18502		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	TYP†	MAX	SN54ABT18502 MIN	MAX	SN74ABT18502 MIN	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = − 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = − 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = − 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V,		CLK, LE, $\overline{OE}$, TCK			±1		±1		±1	µA
	V_I = V_{CC} or GND		A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			−160		−160		−160	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{OFF}	V_{CC} = 0,	V_I or V_O ≤ 5.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V,	A or B ports	Outputs high			4		4		4	mA
	I_O = 0,		Outputs low			80		80		80	
	V_I = V_{CC} or GND		Outputs disabled			4		4		4	
ΔI_{CC}¶	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

NOTE 4: Preliminary specifications based on SPICE analysis
† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

			SN54ABT18502 MIN	SN54ABT18502 MAX	SN74ABT18502 MIN	SN74ABT18502 MAX	UNIT
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low			3		ns
		LEAB or LEBA high			3		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑			5		ns
		A before LEAB↓ or B before LEBA↓			4		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑			0		ns
		A after LEAB↓ or B after LEBA↓			1		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

			SN54ABT18502 MIN	SN54ABT18502 MAX	SN74ABT18502 MIN	SN74ABT18502 MAX	UNIT
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			5		ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑			5		ns
		TDI before TCK↑			6		
		TMS before TCK↑			6		
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑			0		ns
		TDI after TCK↑			0		
		TMS after TCK↑			0		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 4: Preliminary specifications based on SPICE analysis

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18502		SN74ABT18502		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						1	6	ns
t_{PHL}								1	6	
t_{PLH}	CLKAB or CLKBA	B or A						2	6	ns
t_{PHL}								2	6	
t_{PLH}	LEAB or LEBA	B or A						1.5	7.5	ns
t_{PHL}								1.5	7.5	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						2	7.5	ns
t_{PZL}								2	7.5	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						2	7.5	ns
t_{PLZ}								2	7.5	

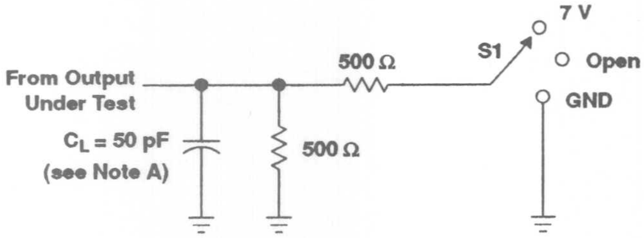
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18502		SN74ABT18502		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						3	12	ns
t_{PHL}								3	12	
t_{PLH}	TCK↓	TDO						2	7	ns
t_{PHL}								2	7	
t_{PZH}	TCK↓	A or B						3	14	ns
t_{PZL}								3	14	
t_{PZH}	TCK↓	TDO						2	8	ns
t_{PZL}								2	8	
t_{PHZ}	TCK↓	A or B						3	14	ns
t_{PLZ}								3	14	
t_{PHZ}	TCK↓	TDO						2	8	ns
t_{PLZ}								2	8	

NOTE 4: Preliminary specifications based on SPICE analysis

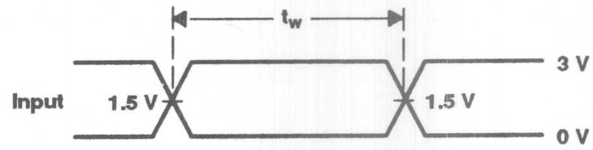
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

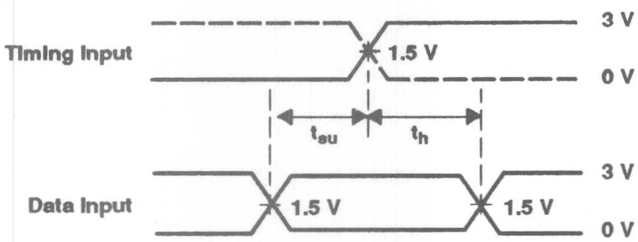


LOAD CIRCUIT FOR OUTPUTS

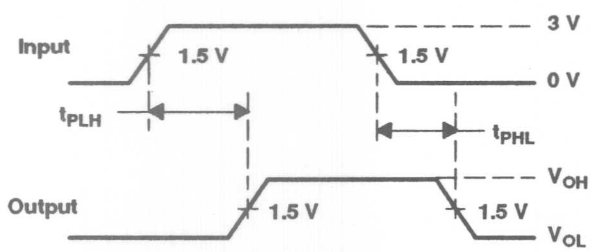
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



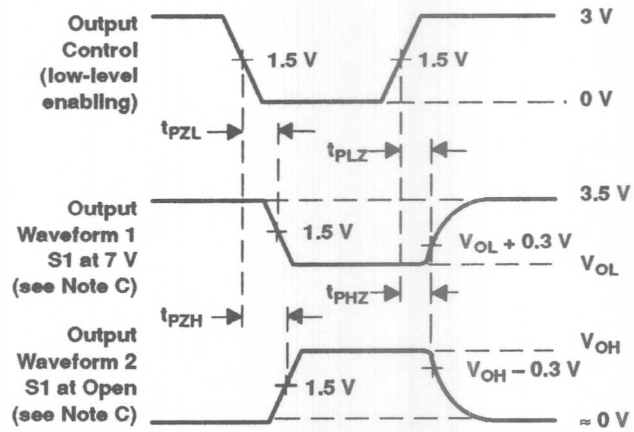
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

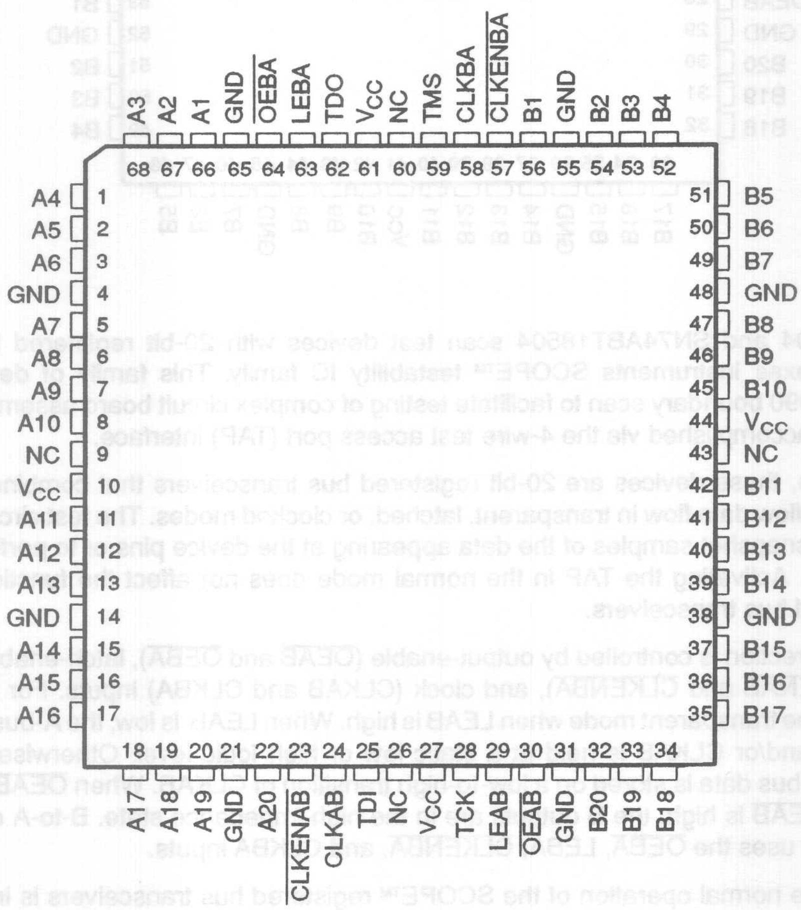
PRODUCT PREVIEW

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (W)

SN54ABT18504 . . . W PACKAGE
(TOP VIEW)



NC – No internal connection

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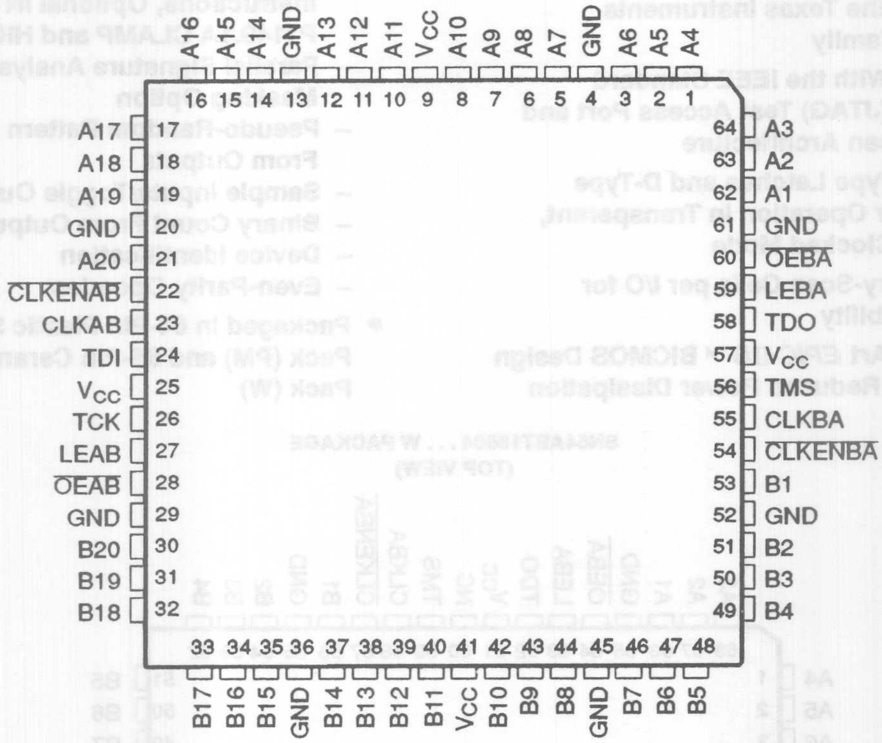
TEXAS INSTRUMENTS

SN74ABT18504 . . . PM PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN54ABT18504 and SN74ABT18504 scan test devices with 20-bit registered bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 20-bit registered bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ registered bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{\text{CLKENAB}}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{\text{CLKENAB}}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{\text{OEAB}}$ is low, the B outputs are active. When $\overline{\text{OEAB}}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{\text{OEBA}}$, LEBA, $\overline{\text{CLKENBA}}$, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ registered bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18504 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT18504 is characterized for operation from −40°C to 85°C.

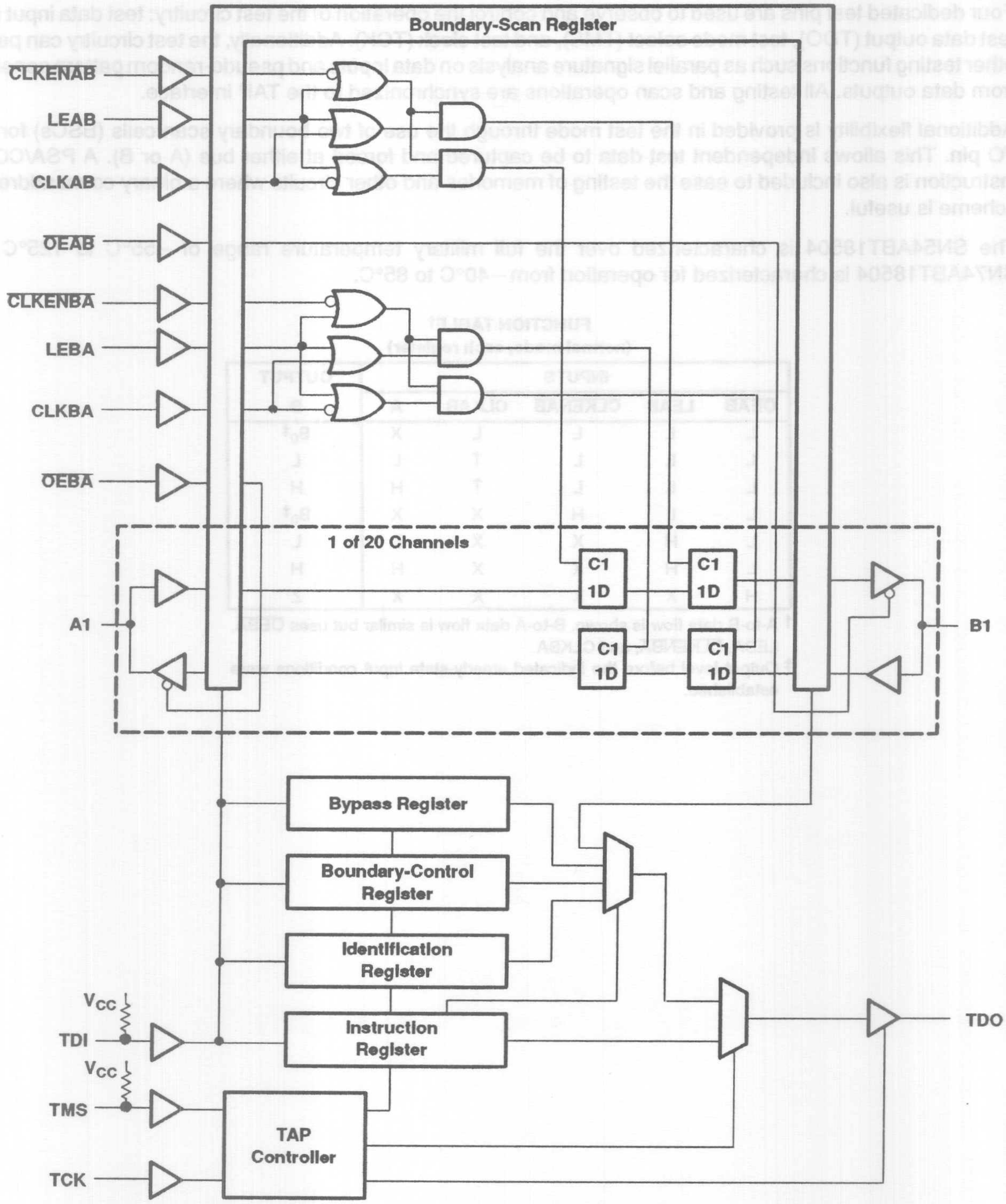
FUNCTION TABLE†
(normal mode, each register)

INPUTS					OUTPUT
$\overline{OEAB}$	LEAB	$\overline{CLKENAB}$	CLKAB	A	B
L	L	L	L	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	H	X	X	B_0‡
L	H	X	X	L	L
L	H	X	X	H	H
H	X	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18504 .... 96 mA
SN74ABT18504 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) (see Note 2) .... 885 mW
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18504 (PM package), the power derating factor for ambient temperatures greater than 55°C is –10.5 mW/°C.

recommended operating conditions (see Note 3)

		SN54ABT18504		SN74ABT18504		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS		T_A = 25°C MIN	TYP†	MAX	SN54ABT18504 MIN	MAX	SN74ABT18504 MIN	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	CLK, CLKEN, LE,OE,TCK			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}	TDI,TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND	TDI,TMS			–160		–160		–160	µA
I_{OZH}‡	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V, V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0, V_I or $V_O \leq$ 5.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND, A or B ports	Outputs high			4		4		4	mA
		Outputs low			88		88		88	
		Outputs disabled			4		4		4	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V	TDO		8						pF

NOTE 4: Preliminary specifications based on SPICE analysis
† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

			SN54ABT18504		SN74ABT18504		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low			3		ns
		LEAB or LEBA high			3		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑			5		ns
		A before LEAB↓ or B before LEBA↓			4		
		$\overline{CLKEN}$ before CLK↑			5		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑			0		ns
		A after LEAB↓ or B after LEBA↓			1		
		$\overline{CLKEN}$ after CLK↑			0		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

			SN54ABT18504		SN74ABT18504		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			5		ns
t_{su}	Setup time	A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ before TCK↑			5		ns
		TDI before TCK↑			6		
		TMS before TCK↑			6		
t_h	Hold time	A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ after TCK↑			0		ns
		TDI after TCK↑			0		
		TMS after TCK↑			0		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 4: Preliminary specifications based on SPICE analysis

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18504		SN74ABT18504		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						1	6	ns
t_{PHL}								1	6	
t_{PLH}	CLKAB or CLKBA	B or A						2	6	ns
t_{PHL}								2	6	
t_{PLH}	LEAB or LEBA	B or A						1.5	7.5	ns
t_{PHL}								1.5	7.5	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						2	7.5	ns
t_{PZL}								2	7.5	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A						2	7.5	ns
t_{PLZ}								2	7.5	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

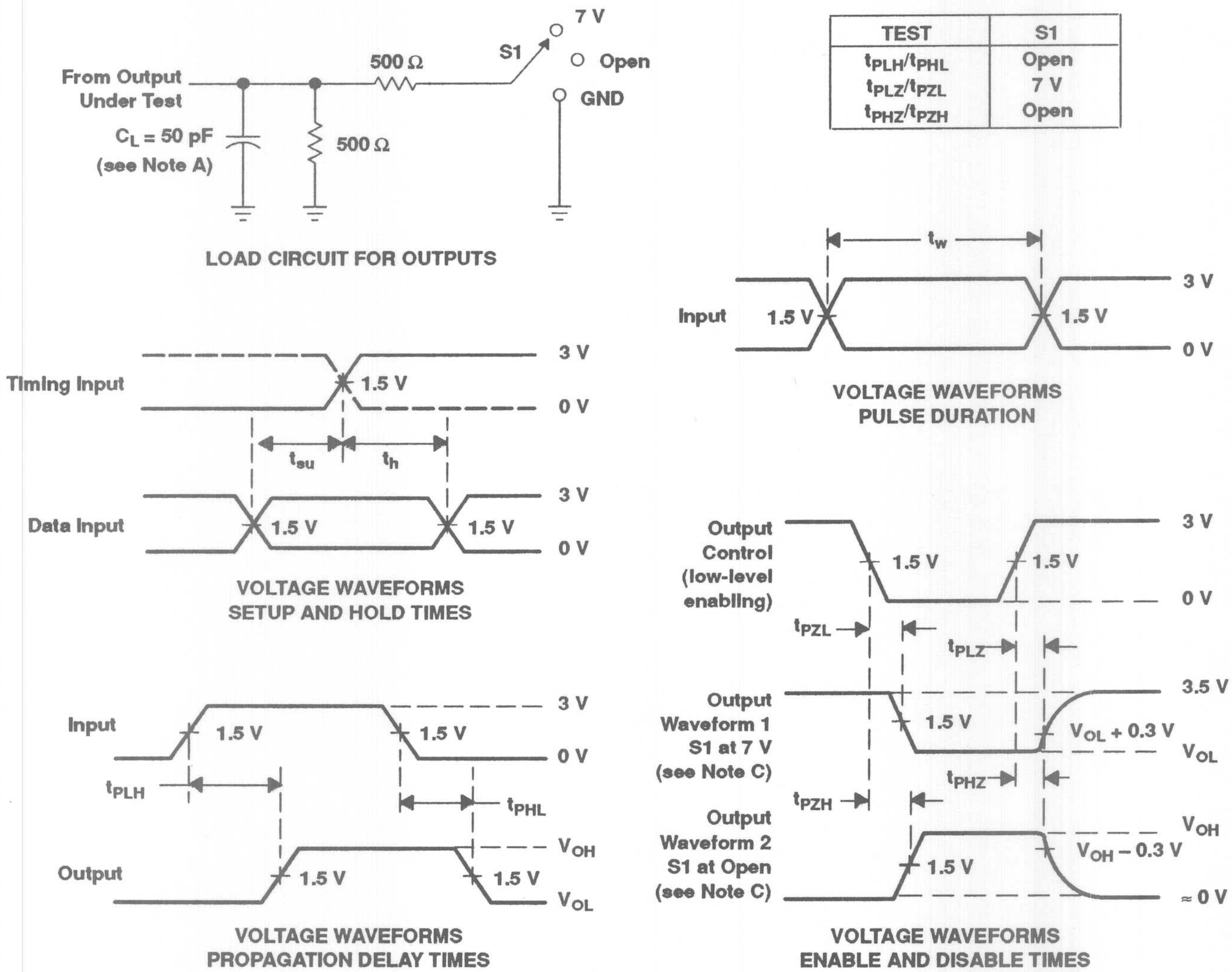
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18504		SN74ABT18504		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						3	12	ns
t_{PHL}								3	12	
t_{PLH}	TCK↓	TDO						2	7	ns
t_{PHL}								2	7	
t_{PZH}	TCK↓	A or B						3	14	ns
t_{PZL}								3	14	
t_{PZH}	TCK↓	TDO						2	8	ns
t_{PZL}								2	8	
t_{PHZ}	TCK↓	A or B						3	14	ns
t_{PLZ}								3	14	
t_{PHZ}	TCK↓	TDO						2	8	ns
t_{PLZ}								2	8	

NOTE 4: Preliminary specifications based on SPICE analysis

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



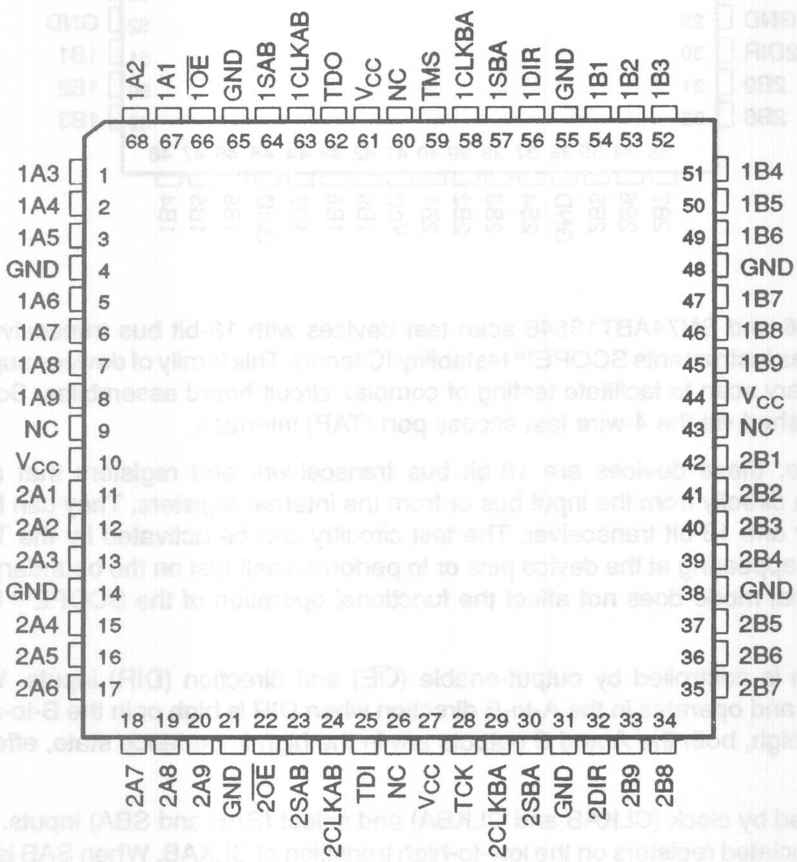
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art *EPIC-IIB*™ BICMOS Design Significantly Reduces Power Dissipation
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (W)

SN54ABT18646 . . . W PACKAGE
(TOP VIEW)



NC – No internal connection

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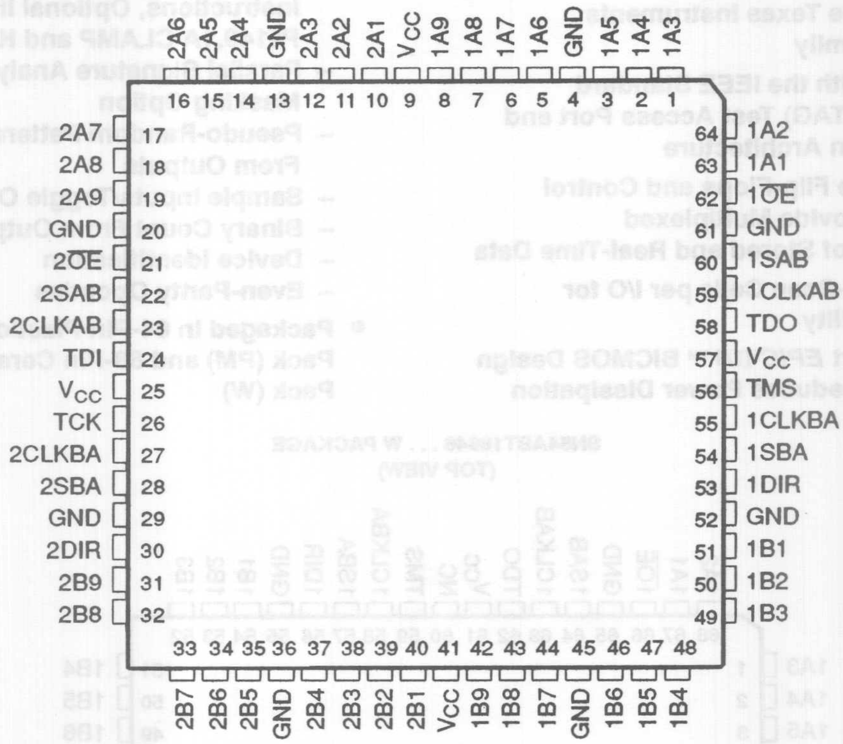
SN74ABT18646 . . . PM PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN54ABT18646 and SN74ABT18646 scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Transceiver function is controlled by output-enable ($\overline{OE}$) and direction (DIR) inputs. When $\overline{OE}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{OE}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that may be performed with the 'ABT18646.

description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18646 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT18646 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input disabled	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input disabled	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

PRODUCT PREVIEW

PRODUCT PREVIEW

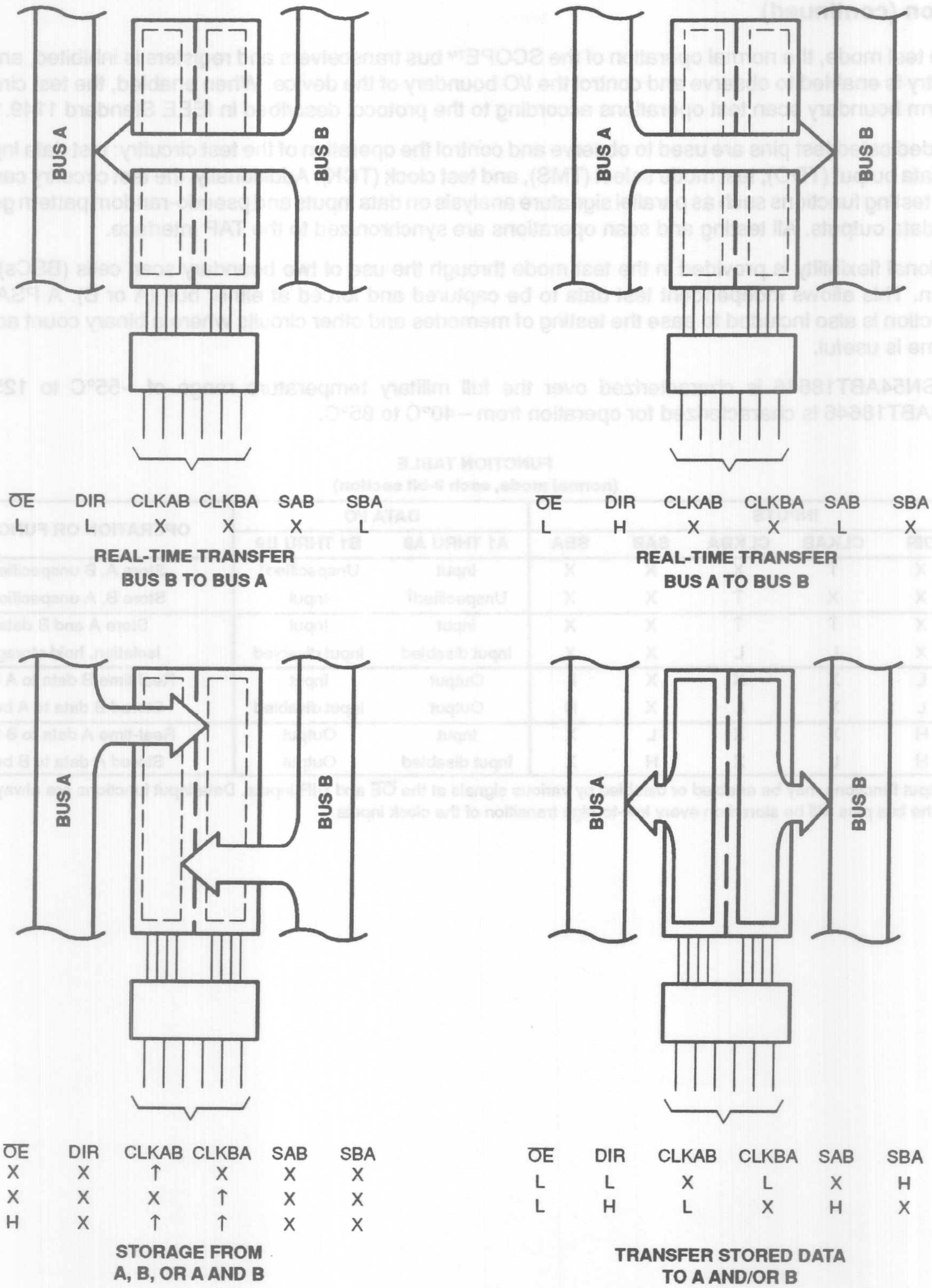
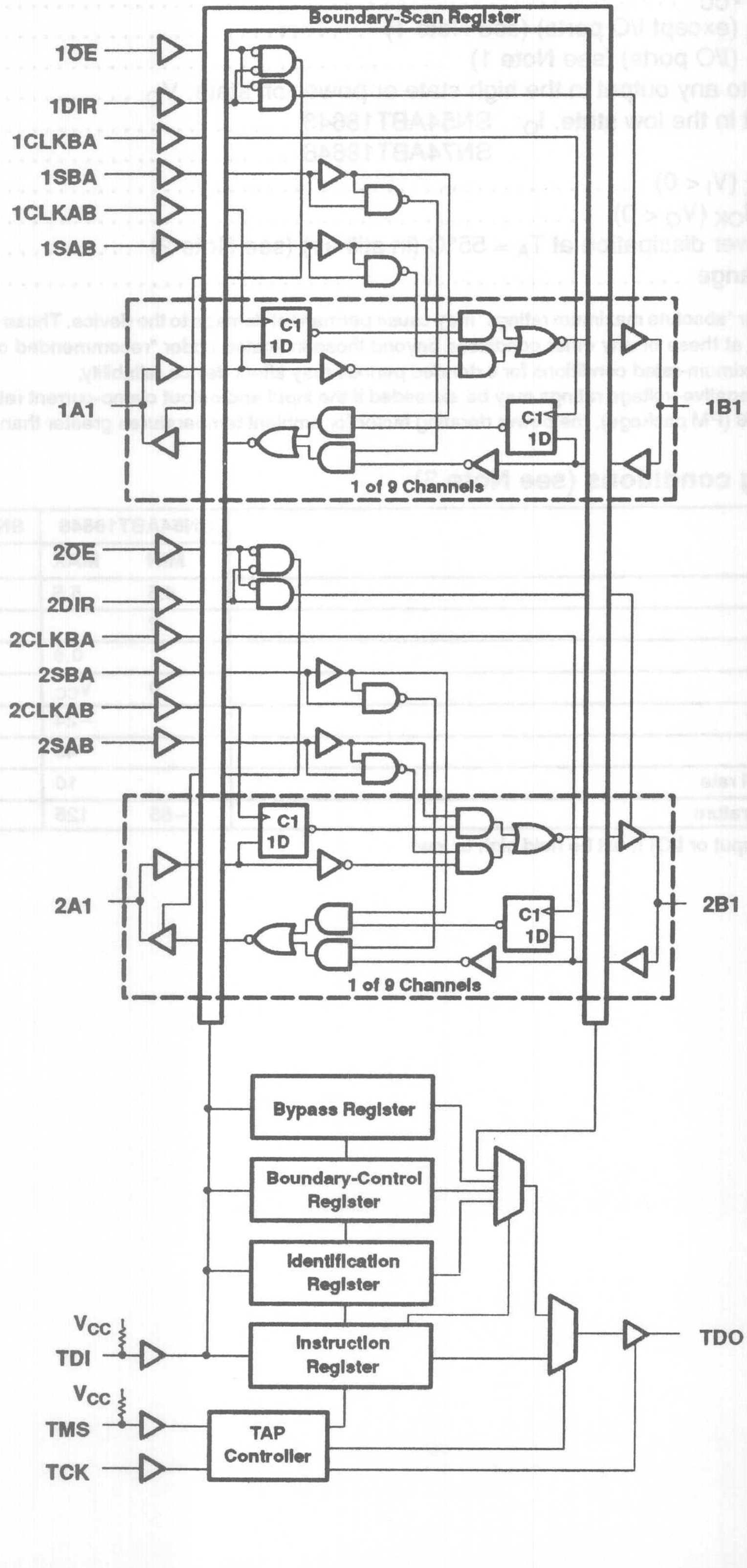


Figure 1. Bus-Management Functions

functional block diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18646 .... 96 mA
SN74ABT18646 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) (see Note 2) .... 885 mW
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18646 (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

recommended operating conditions (see Note 3)

		SN54ABT18646		SN74ABT18646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS		$T_A = 25°C$			SN54ABT18646		SN74ABT18646		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA				−1.2		−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -3$ mA		2.5			2.5		2.5		V
	$V_{CC} = 5$ V, $I_{OH} = -3$ mA		3			3		3		
	$V_{CC} = 4.5$ V, $I_{OH} = -24$ mA		2			2				
	$V_{CC} = 4.5$ V, $I_{OH} = -32$ mA		2*					2		
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 48$ mA				0.55		0.55			V
	$V_{CC} = 4.5$ V, $I_{OL} = 64$ mA				0.55*				0.55	
I_I	$V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND	CLK, DIR, $\overline{OE}$, S, TCK			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{IH}	$V_{CC} = 5.5$ V, $V_I = V_{CC}$	TDI, TMS			10		10		10	µA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = GND$	TDI, TMS			−160		−160		−160	µA
I_{OZH}‡	$V_{CC} = 5.5$ V, $V_O = 2.7$ V				50		50		50	µA
I_{OZL}‡	$V_{CC} = 5.5$ V, $V_O = 0.5$ V				−50		−50		−50	µA
I_{OFF}	$V_{CC} = 0$, V_I or $V_O \le 5.5$ V				±100		±450		±100	µA
I_{CEX}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O§	$V_{CC} = 5.5$ V, $V_O = 2.5$ V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND, A or B ports	Outputs high		0.9	2		2		2	mA
		Outputs low		30	38		38		38	
		Outputs disabled		0.9	2		2		2	
ΔI_{CC}¶	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	$V_I = 2.5$ V or 0.5 V	Control inputs		3						pF
C_{io}	$V_O = 2.5$ V or 0.5 V	A or B ports		10						pF
C_o	$V_O = 2.5$ V or 0.5 V	TDO		8						pF

NOTE 4: Preliminary specifications based on SPICE analysis
† All typical values are at $V_{CC} = 5$ V.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

			SN54ABT18646		SN74ABT18646		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low			3		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑			5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑			0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

			SN54ABT18646		SN74ABT18646		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			5		ns
t_{su}	Setup time	A, B, CLK, DIR, $\overline{OE}$, or S before TCK↑			5		ns
		TDI before TCK↑			6		
		TMS before TCK↑			6		
t_h	Hold time	A, B, CLK, DIR, $\overline{OE}$, or S after TCK↑			0		ns
		TDI after TCK↑			0		
		TMS after TCK↑			0		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 4: Preliminary specifications based on SPICE analysis

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18646		SN74ABT18646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						1	6	ns
t_{PHL}								1	6	
t_{PLH}	CLKAB or CLKBA	B or A						2	6	ns
t_{PHL}								2	6	
t_{PLH}	SAB or SBA	B or A						2	8	ns
t_{PHL}								2	8	
t_{PZH}	DIR	B or A						2	7.5	ns
t_{PZL}								2	7.5	
t_{PZH}	$\overline{OE}$	B or A						2	7.5	ns
t_{PZL}								2	7.5	
t_{PHZ}	DIR	B or A						2	7.5	ns
t_{PLZ}								2	7.5	
t_{PHZ}	$\overline{OE}$	B or A						2	7.5	ns
t_{PLZ}								2	7.5	

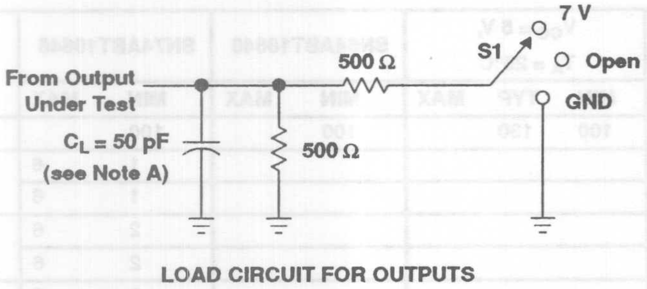
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18646		SN74ABT18646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						3	12	ns
t_{PHL}								3	12	
t_{PLH}	TCK↓	TDO						2	7	ns
t_{PHL}								2	7	
t_{PZH}	TCK↓	A or B						3	14	ns
t_{PZL}								3	14	
t_{PZH}	TCK↓	TDO						2	8	ns
t_{PZL}								2	8	
t_{PHZ}	TCK↓	A or B						3	14	ns
t_{PLZ}								3	14	
t_{PHZ}	TCK↓	TDO						2	8	ns
t_{PLZ}								2	8	

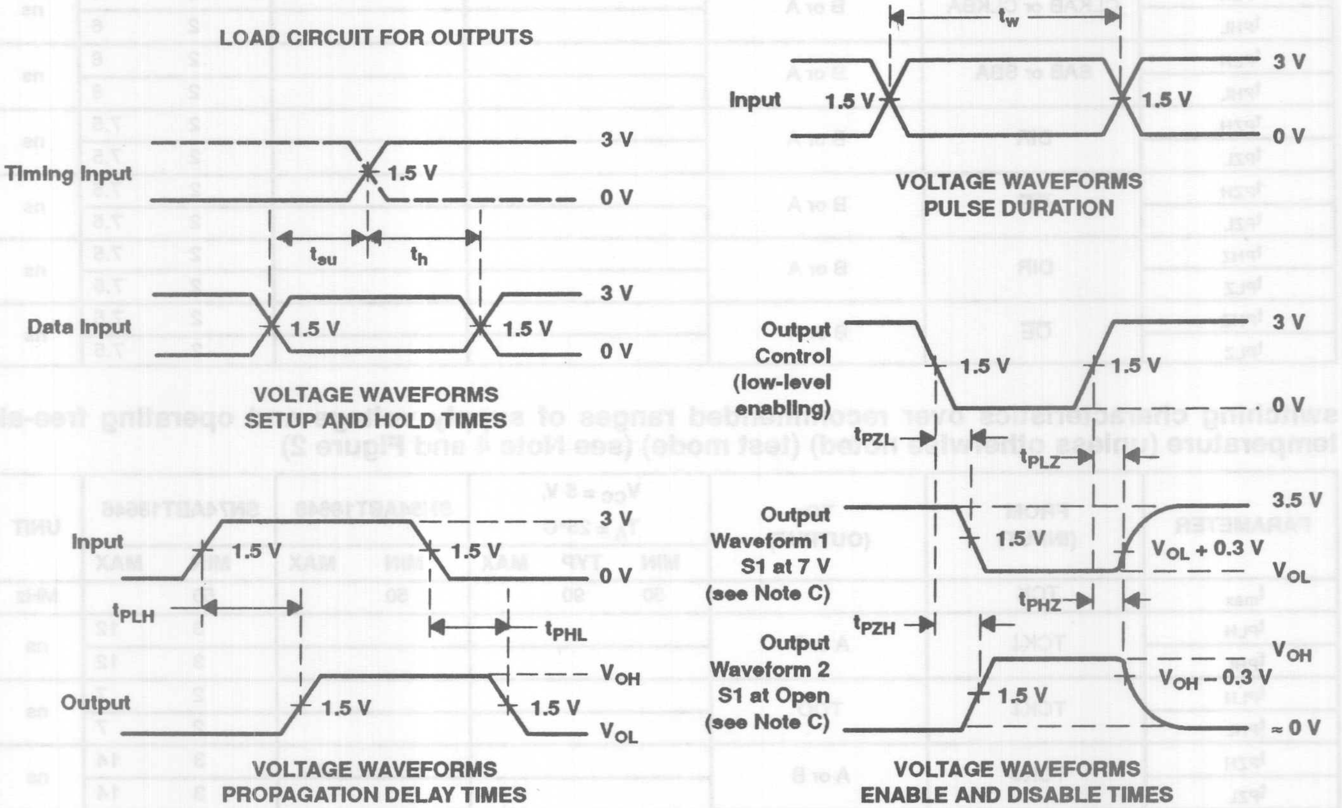
NOTE 4: Preliminary specifications based on SPICE analysis

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



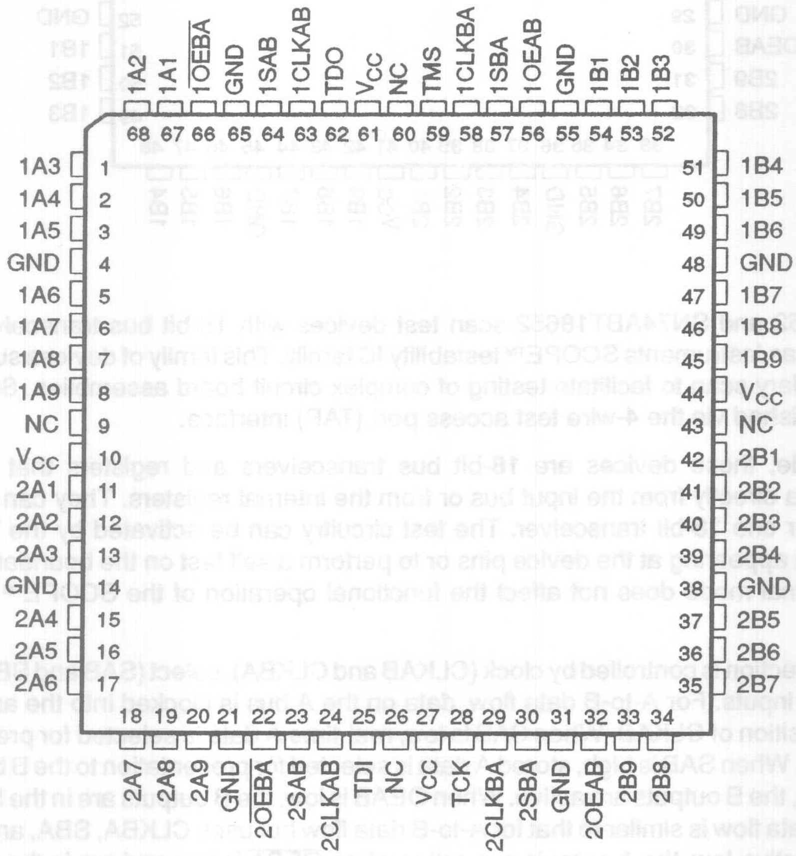
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-ⅡB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (W)**

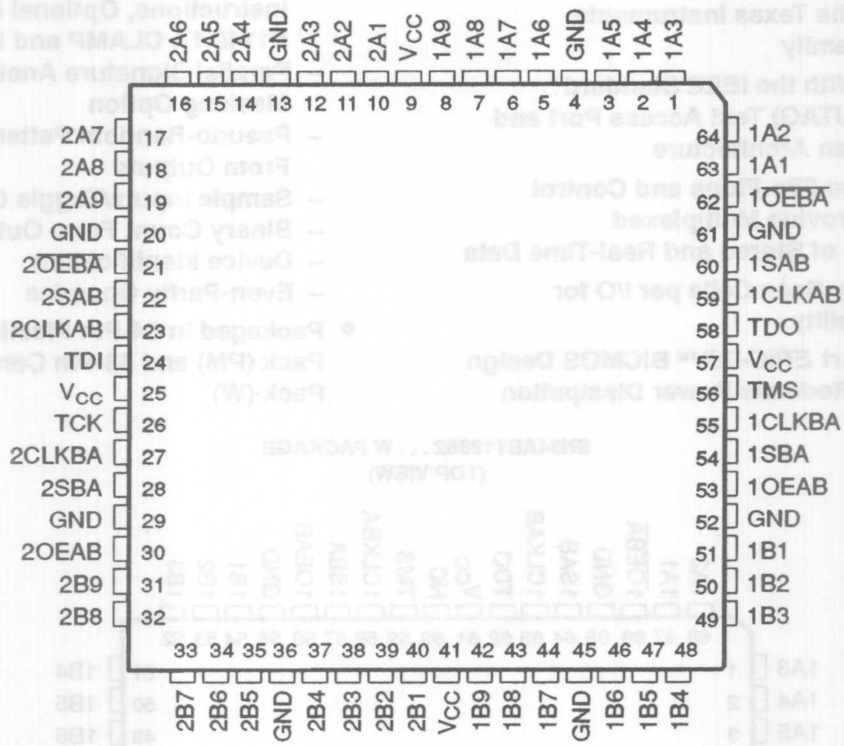
SN54ABT18652 . . . W PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

SN74ABT18652 . . . PM PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN54ABT18652 and SN74ABT18652 scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and $\overline{\text{OEBA}}$ inputs. Since the $\overline{\text{OEBA}}$ input is active-low, the A outputs are active when $\overline{\text{OEBA}}$ is low and are in the high-impedance state when $\overline{\text{OEBA}}$ is high. Figure 1 illustrates the four fundamental bus-management functions that may be performed with the ’ABT18652.

description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18652 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT18652 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	
L	H	L	L	X	X	Input disabled	Input disabled	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

PRODUCT PREVIEW

PRODUCT PREVIEW

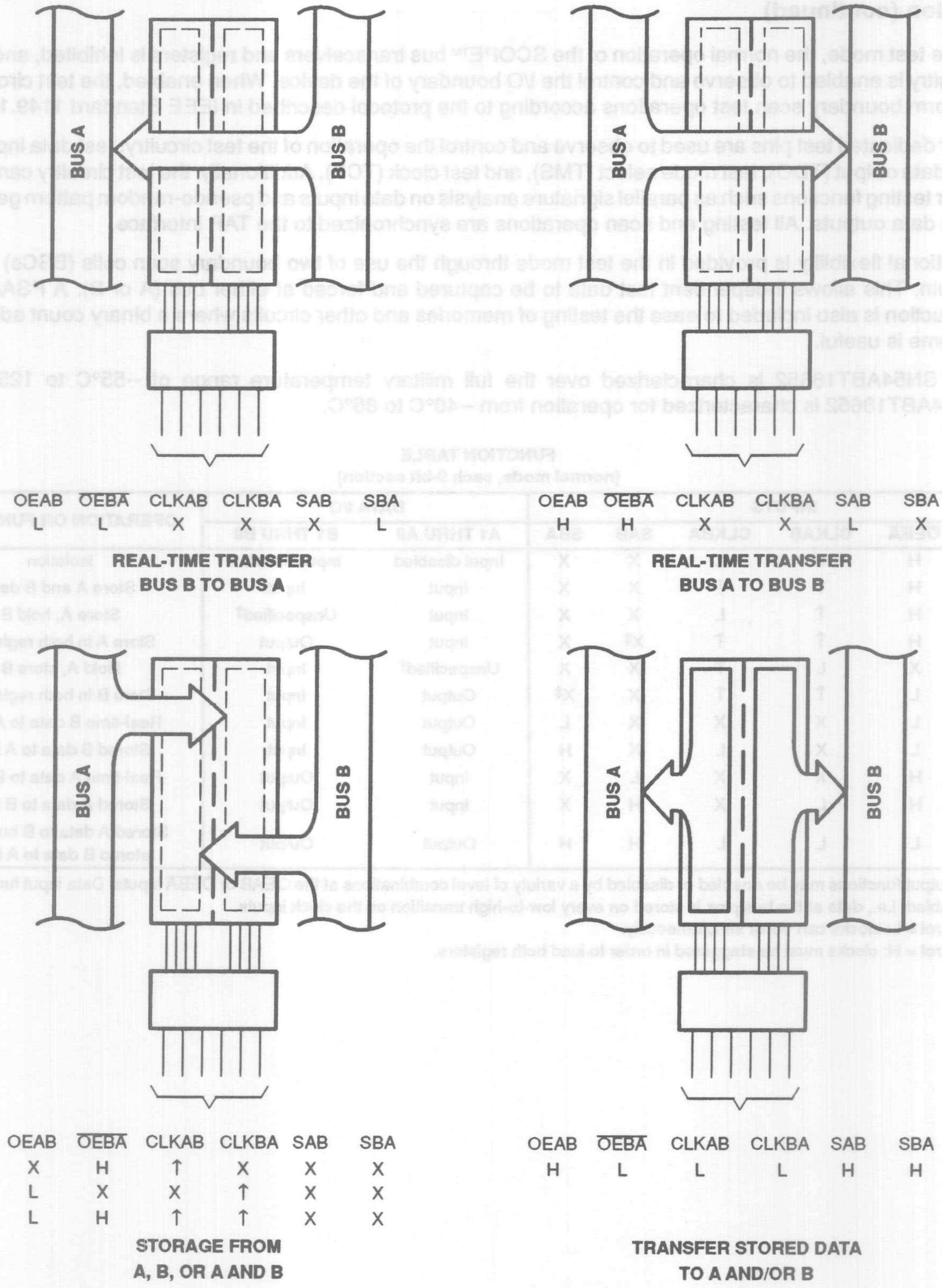
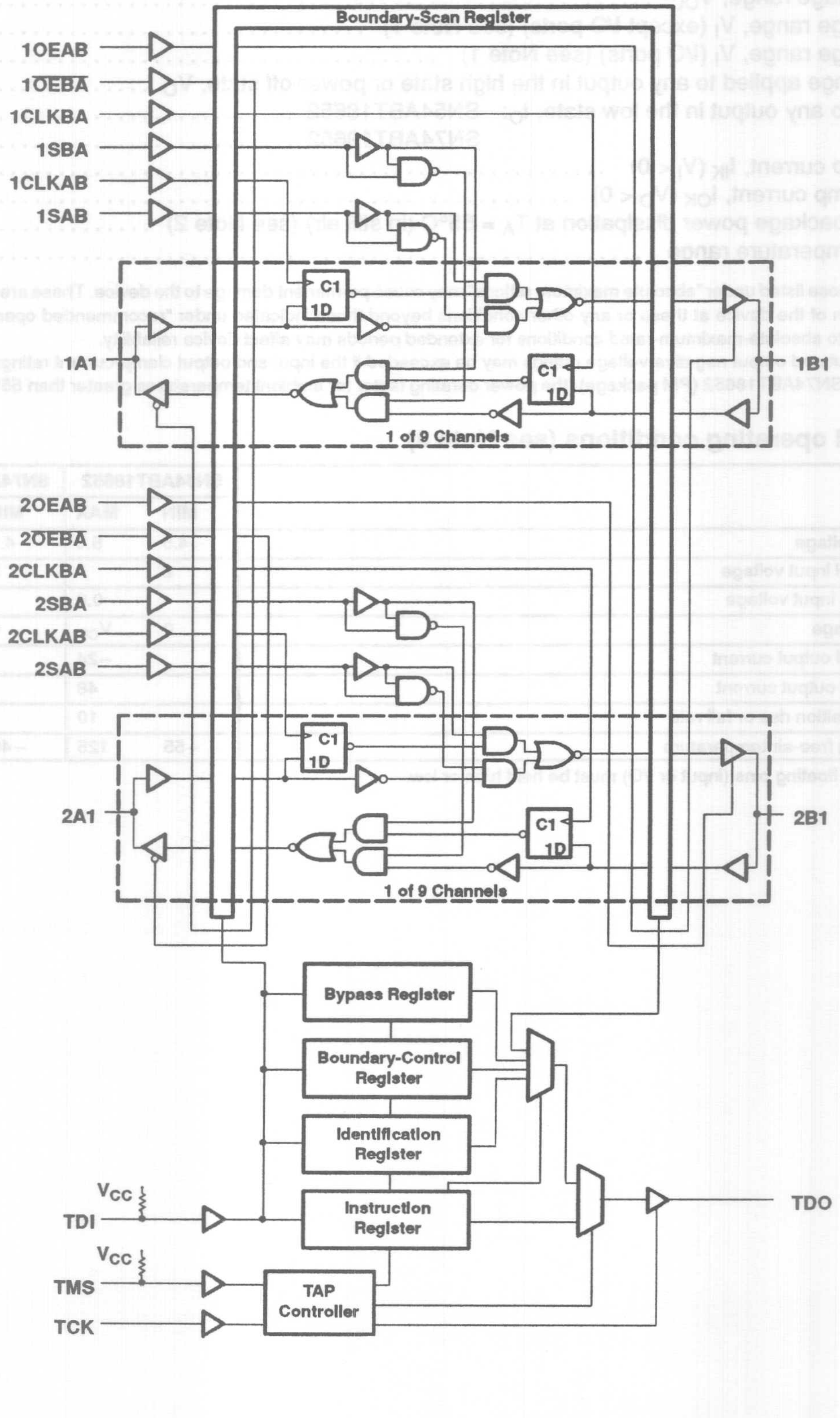


Figure 1. Bus-Management Functions

functional block diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18652 .... 96 mA
SN74ABT18652 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) (see Note 2) .... 885 mW
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18652 (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

recommended operating conditions (see Note 3)

		SN54ABT18652		SN74ABT18652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS		T_A = 25°C MIN	T_A = 25°C TYP†	T_A = 25°C MAX	SN54ABT18652 MIN	SN54ABT18652 MAX	SN74ABT18652 MIN	SN74ABT18652 MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = − 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = − 3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = − 24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = − 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	CLK, OEAB, $\overline{OEBA}$, S, TCK			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND	TDI, TMS			−160		−160		−160	µA
I_{OZH}‡	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{OFF}	V_{CC} = 0, V_I or V_O ≤ 5.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND, A or B ports	Outputs high			4		4		4	mA
		Outputs low			80		80		80	
		Outputs disabled			4		4		4	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V	TDO		8						pF

NOTE 4: Preliminary specifications based on SPICE analysis

† All typical values are at V_{CC} = 5 V.

‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

			SN54ABT18652 MIN	SN54ABT18652 MAX	SN74ABT18652 MIN	SN74ABT18652 MAX	UNIT
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low			3		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑			5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑			0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

			SN54ABT18652 MIN	SN54ABT18652 MAX	SN74ABT18652 MIN	SN74ABT18652 MAX	UNIT
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			5		ns
t_{su}	Setup time	A, B, CLK, OEAB, $\overline{OEBA}$, or S before TCK↑			5		ns
		TDI before TCK↑			6		
		TMS before TCK↑			6		
t_h	Hold time	A, B, CLK, OEAB, $\overline{OEBA}$, or S after TCK↑			0		ns
		TDI after TCK↑			0		
		TMS after TCK↑			0		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 4: Preliminary specifications based on SPICE analysis

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18652		SN74ABT18652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						1	6	ns
t_{PHL}								1	6	
t_{PLH}	CLKAB or CLKBA	B or A						2	6	ns
t_{PHL}								2	6	
t_{PLH}	SAB or SBA	B or A						2	8	ns
t_{PHL}								2	8	
t_{PZH}	OEAB or $\overline{\text{OEBA}}$	B or A						2	7.5	ns
t_{PZL}								2	7.5	
t_{PHZ}	OEAB or $\overline{\text{OEBA}}$	B or A						2	7.5	ns
t_{PLZ}								2	7.5	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18652		SN74ABT18652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						3	12	ns
t_{PHL}								3	12	
t_{PLH}	TCK↓	TDO						2	7	ns
t_{PHL}								2	7	
t_{PZH}	TCK↓	A or B						3	14	ns
t_{PZL}								3	14	
t_{PZH}	TCK↓	TDO						2	8	ns
t_{PZL}								2	8	
t_{PHZ}	TCK↓	A or B						3	14	ns
t_{PLZ}								3	14	
t_{PHZ}	TCK↓	TDO						2	8	ns
t_{PLZ}								2	8	

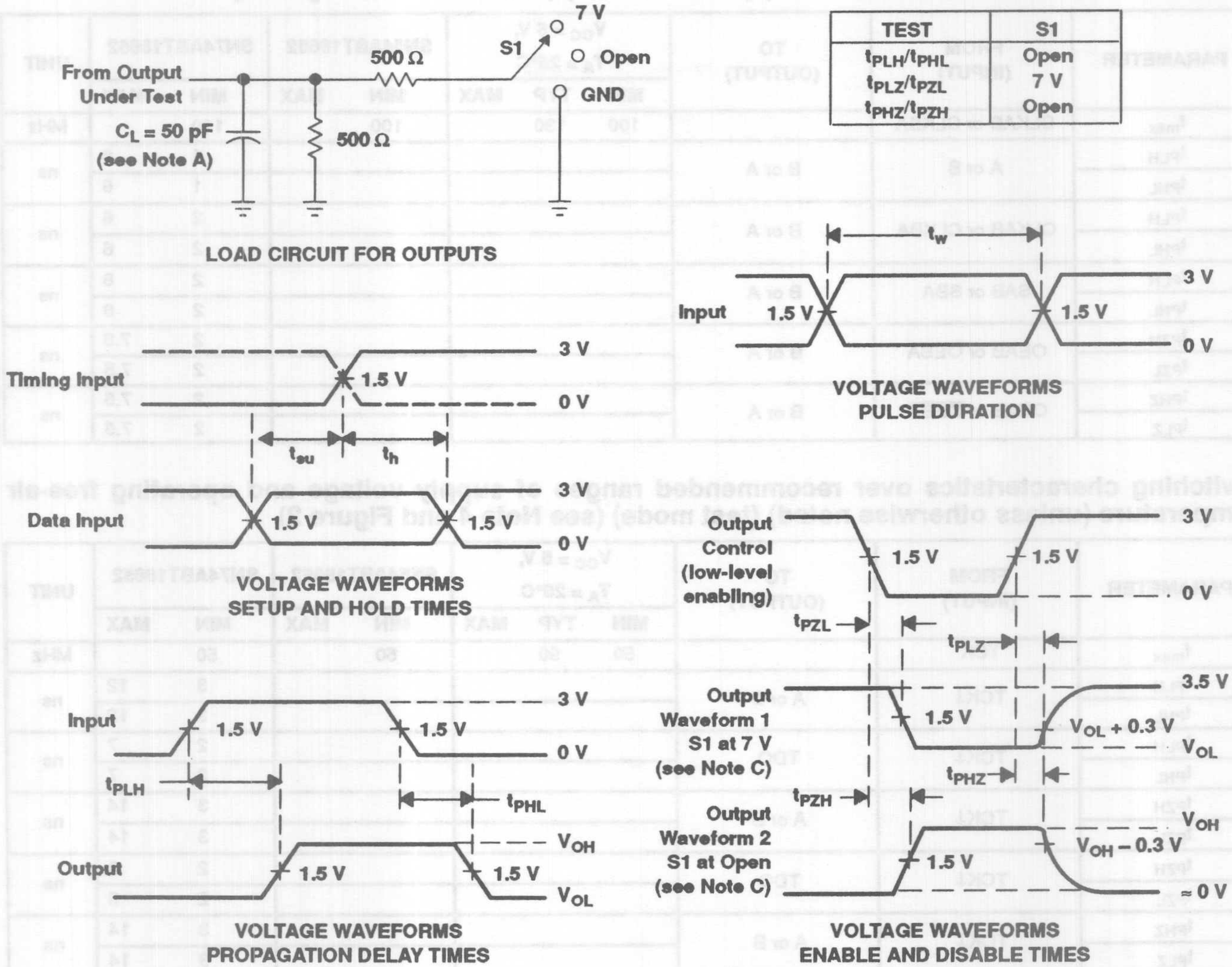
NOTE 4: Preliminary specifications based on SPICE analysis

PRODUCT PREVIEW

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_0 = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Control Operation of up to Six Parallel Target Scan Paths
- Accommodate Pipeline Delay to Target of up to 31 Clock Cycles
- Scan Data for up to 2^{32} Clock Cycles
- Execute Instructions for up to 2^{32} Clock Cycles
- Each Includes Four Bidirectional Event Pins for Additional Test Capability
- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Packaged in 44-pin Plastic Leaded Chip Carrier (FN) and 68-pin Ceramic Quad Flat Pack (W)

description

The 'ACT8990 test bus controller (TBC) is a member of the Texas Instruments SCOPE™ testability IC family. This family of components supports IEEE Standard 1149.1-1990 (JTAG) boundary scan to facilitate testing of complex circuit board assemblies. The 'ACT8990 differs from other SCOPE™ ICs in that, rather than being a boundary-scannable device, its function is to control the JTAG serial test bus.

The required signals of the JTAG serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), and test data output (TDO) – may be connected from the TBC to a target device (a chain of IEEE Standard 1149.1-1990 boundary-scannable components that share the same serial test bus) without the need for additional logic. The TBC generates TMS and TDI signals for its target(s), receives TDO signals from its target(s), and buffers its TCK input (TCKI) to a TCK output (TCKO) for distribution to its target(s). The TMS, TDI, and TDO signals may be connected to a target directly or via a pipeline with a retiming delay of up to 31 bits. Since the TBC can be configured to generate up to six separate TMS signals (TMS5–0), it may be used to control up to six target devices that are connected in parallel (i.e., sharing common TCK, TDI, and TDO signals).

While most operations of the TBC are synchronous to TCKI, a test off ($\overline{\text{TOFF}}$) pin is provided for output control of the target interface, and a test reset ($\overline{\text{TRST}}$) pin is provided for hardware/software reset of the TBC. In addition, four event (EVENT3–0) I/O pins are provided for asynchronous communication to target device(s). Each event pin has its own event generation/detection logic, and detected events may be counted by two 16-bit counters.

The TBC operates under the control of a host microprocessor/microcontroller via the 5-bit address bus ADRS(4–0) and the 16-bit read/write data bus DATA(15–0). Read ($\overline{\text{RD}}$) and write ($\overline{\text{WR}}$) strobes are implemented such that the critical host interface timing is independent of the TCKI period. Any of 24 registers may be addressed for read and/or write operations. In addition to control and status registers, the TBC contains two command registers, a read buffer, and a write buffer. Status of the TBC is transmitted to the host via ready ($\overline{\text{RDY}}$) and interrupt ($\overline{\text{INT}}$) pins.

Major commands may be issued by the host to cause the TBC to generate the TMS sequences necessary to move the target(s) from any stable test access port (TAP) controller state to any other stable TAP state, to execute instructions in the Run-Test/Idle TAP state, or to scan instruction or test data through the target(s). A 32-bit counter may be preset to allow a predetermined number of execution or scan operations.

Serial data that appears at the selected TDI input (TDI1 or TDI0) is transferred into the read buffer, which may be read by the host to obtain up to 16 bits of the serial data stream. Serial data to be transmitted from the TDO output is written by the host to the write buffer.

The SN54ACT8990 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ACT8990 is characterized for operation from 0°C to 70°C.

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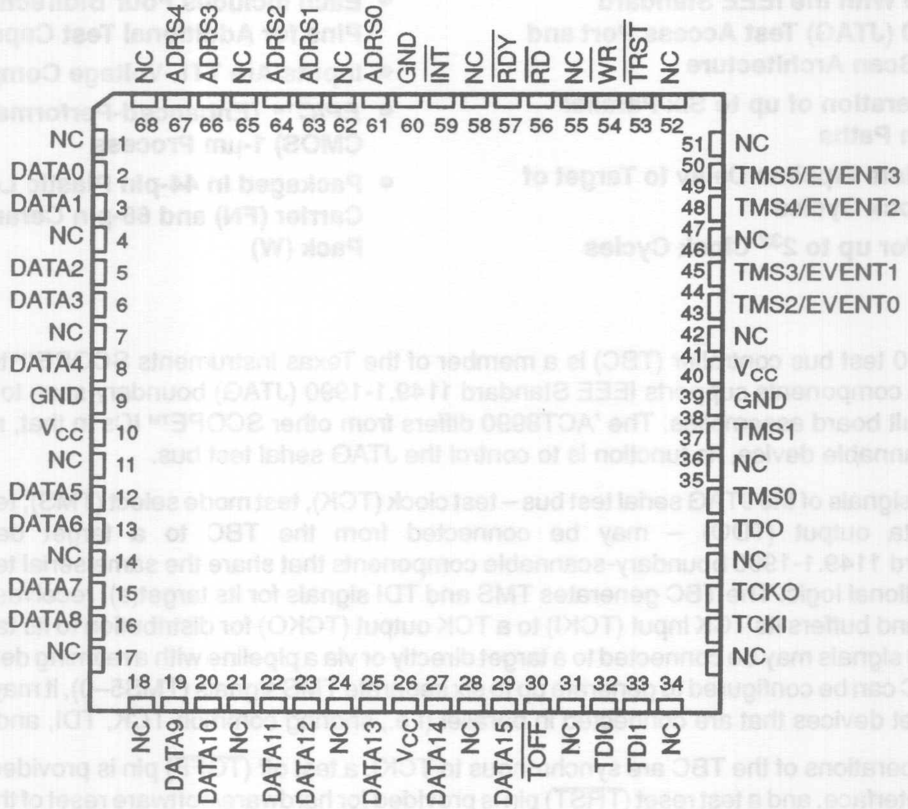
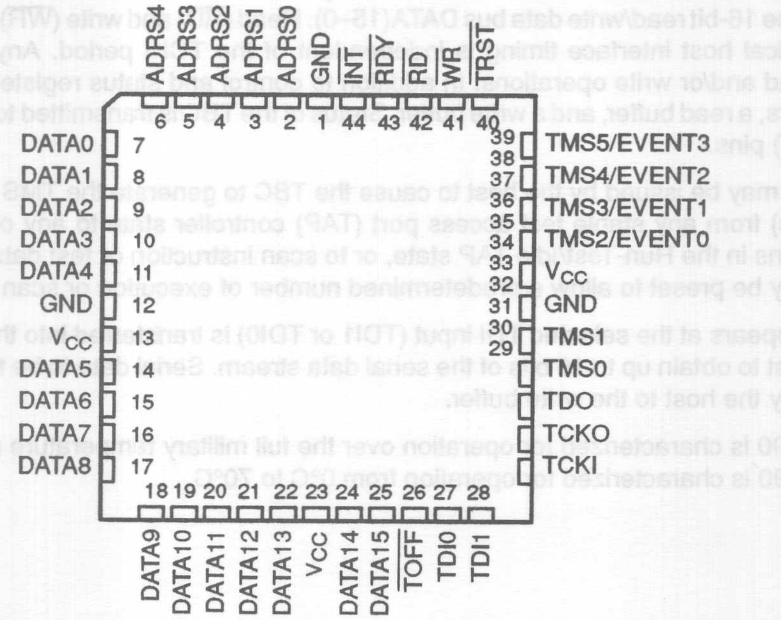
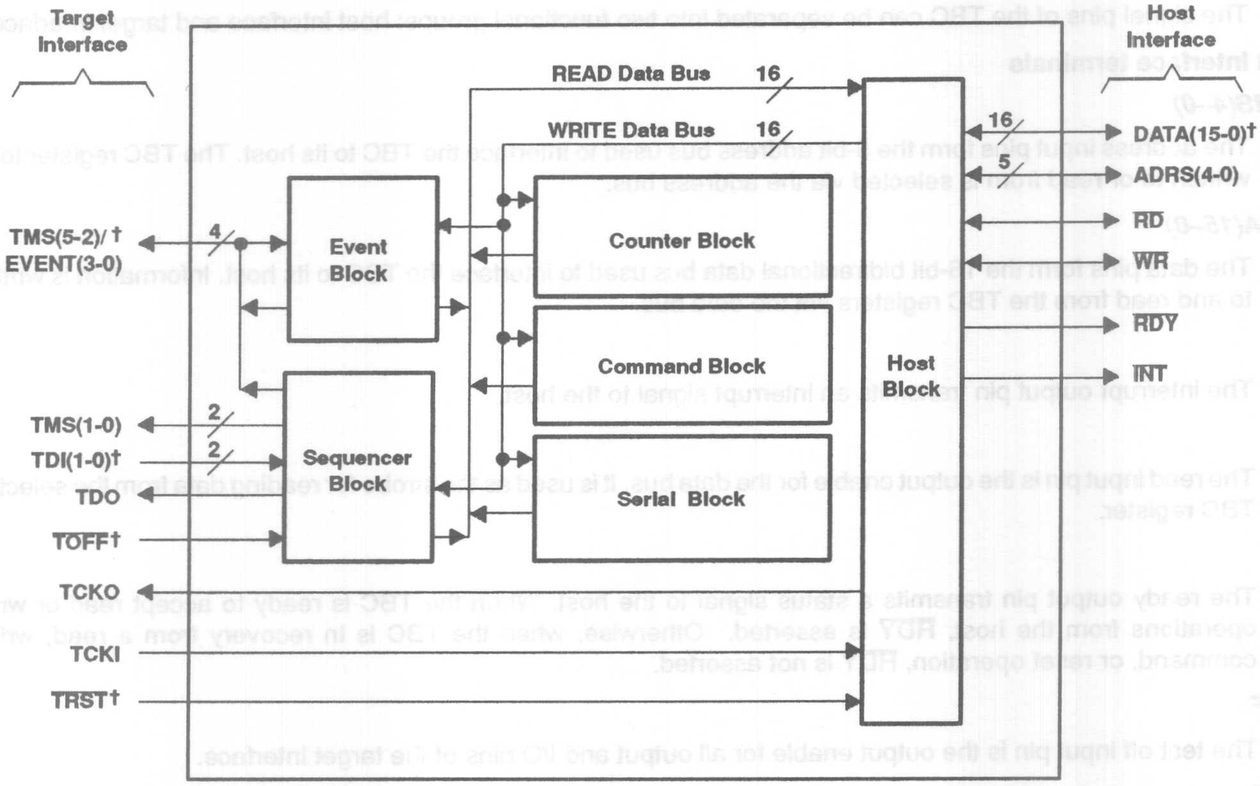
SN54ACT8990 . . . W PACKAGE
(TOP VIEW)



SN74ACT8990 . . . FN PACKAGE
(TOP VIEW)



functional block diagram



† Inputs have internal pullup resistors.

terminal functions

PIN NAME	GROUP	TYPE	DESCRIPTION
ADRS(4-0)	Host Interface	Input	Address Bus
DATA(15-0)		I/O	Data Bus
INT		Output	Interrupt
RD		Input	Read Strobe
RDY		Output	Ready
WR		Input	Write Strobe
TCKI	Target Interface	Input	Test Clock Input
TCKO		Output	Test Clock Output
TDI(1-0)		Input	Test Data Input
TDO		Output	Test Data Output
TMS(1-0)		Output	Test Mode Select
TMS(5-2)/EVENT(3-0)		I/O	Test Mode Select/Event
TOFF		Input	Test Off
TRST		Input	Test Reset

terminal descriptions

The signal pins of the TBC can be separated into two functional groups: host interface and target interface.

host interface terminals

ADRS(4–0)

The address input pins form the 5-bit address bus used to interface the TBC to its host. The TBC register to be written to or read from is selected via the address bus.

DATA(15–0)

The data pins form the 16-bit bidirectional data bus used to interface the TBC to its host. Information is written to and read from the TBC registers via the data bus.

$\overline{INT}$

The interrupt output pin transmits an interrupt signal to the host.

$\overline{RD}$

The read input pin is the output enable for the data bus. It is used as the strobe for reading data from the selected TBC register.

$\overline{RDY}$

The ready output pin transmits a status signal to the host. When the TBC is ready to accept read or write operations from the host, $\overline{RDY}$ is asserted. Otherwise, when the TBC is in recovery from a read, write, command, or reset operation, $\overline{RDY}$ is not asserted.

$\overline{TOFF}$

The test off input pin is the output enable for all output and I/O pins of the target interface.

$\overline{TRST}$

The test reset input pin is used to initiate hardware and software reset operations of the TBC. Hardware reset begins when $\overline{TRST}$ is asserted. Software reset begins when $\overline{TRST}$ is released and proceeds synchronously to the test clock input (TCKI), completing in a predetermined number of cycles.

$\overline{WR}$

The write input pin is the strobe for writing data to a TBC data register. Signals present at the data and address buses are captured on the rising edge of $\overline{WR}$.

target interface terminals

TCKI

The test clock input pin is the clock input for the TBC. Most operations of the TBC are synchronous to TCKI. When enabled, all target interface outputs change on the falling edge of TCKI. Sampling of target interface inputs may be configured to occur on either the rising edge or falling edge of TCKI.

TCKO

The test clock output pin distributes the test clock to the target(s). The TCKO pin may be configured to be disabled, constant zero, constant one, or to follow TCKI. When TCKO follows TCKI, it delays the test clock signal to match the delay of generating the test data output (TDO) and test mode select (TMS) signals.

TDI(1–0)

The test data input pins are the serial inputs for shifting test data from the target(s). The TDI inputs may be directly connected to the TDO pin(s) of the target(s).

terminal descriptions (continued)

TDO

The test data output pin is the serial output for shifting test data into the target(s). The TDO output may be directly connected to the TDI pin(s) of the target(s).

TMS(1–0)

The test mode select output pins transmit TMS signals to the target(s), thereby directing them through their test access port (TAP) controller states. The TMS outputs may be directly connected to the TMS pins of the target(s).

TMS(5–2)/EVENT(3–0)

The test mode select/event pins may be configured for use as either test mode select outputs or event I/O pins. As test mode select outputs, they function similarly to the TMS1–0 pins above. As event I/O pins, they can be used to receive/transmit interrupt signals to/from the target(s).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC}
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		SN54ACT8990		SN74ACT8990		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
T_A	Operating free-air temperature	–55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	TYP†	MAX	SN54ACT8990 MIN	MAX	SN74ACT8990 MIN	MAX	UNIT
V_{OH}		I_{OH} = −20 µA	4.5 V	4.4			4.4		4.4		V
		I_{OH} = − 8 mA		3.7			3.7		3.7		
		I_{OH} = −20 µA	4.5 V	5.4			5.4		5.4		
		I_{OH} = −8 mA		4.7			4.7		4.7		
V_{OL}		I_{OL} = 20 µA	4.5 V to 5.5 V			0.1		0.1		0.1	V
		I_{OL} = 8 mA				0.5		0.5		0.5	
I_I	ADRS, $\overline{RD}$, $\overline{WR}$, TCKI	V_I = V_{CC} or GND	5.5 V			±1		±1		±1	µA
	TDI, TOFF, $\overline{TRST}$	V_I = V_{CC}	5.5 V			±1		±1		±1	
		V_I = GND			−70	±250		±250		±250	
I_{OZ}‡	$\overline{INT}$, $\overline{RDY}$, TCKO, TDO, TMS	V_O = V_{CC} or GND	5.5 V			±10		±10		±10	µA
	DATA, TMS/EVENT	V_O = V_{CC}	5.5 V			±10		±10		±10	
		V_O = GND			−70	±250		±250		±250	
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V					450		450	µA

† Typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

			SN54ACT8990 MIN	MAX	SN74ACT8990 MIN	MAX	UNIT
f_{clock}	Clock frequency			30		30	MHz
t_w	Pulse duration	$\overline{WR}$ low	5.5		5.5		ns
		EVENT high or low	8		8		
		TCKI high or low	10.5		10.5		
		$\overline{TRST}$ low	6		6		
t_{su}	Setup time	ADRS before $\overline{WR}$↑	6.5		6.5		ns
		DATA before $\overline{WR}$↑	6		6		
		EVENT before TCKI↑	6		5.5		
		EVENT before TCKI↓	5		5		
		TDI before TCKI↑	2		2		
		TDI before TCKI↓	2		2		
t_h	Hold time	ADRS after $\overline{WR}$↑	5.5		5		ns
		DATA after $\overline{WR}$↑	5.5		5.5		
		EVENT after TCKI↑	5.5		5		
		EVENT after TCKI↓	5		5		
		TDI after TCKI↑	2.5		2.5		
		TDI after TCKI↓	2.5		2.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

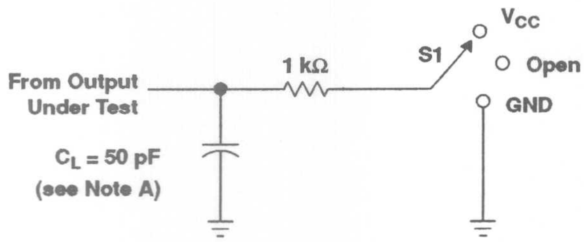
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8990 MIN	SN54ACT8990 MAX	SN74ACT8990 MIN	SN74ACT8990 MAX	UNIT
f_{max}			30		30		MHz
t_{PLH}	ADRS	DATA	19.5	40.5	19.5	39.3	ns
t_{PHL}			19.5	40.5	19.5	39.3	
t_{PLH}	$\overline{RD}\uparrow$	$\overline{RDY}$	5.3	14.4	5.3	13.8	ns
t_{PLH}	$\overline{WR}\uparrow$	$\overline{RDY}$	2.5	13.6	2.5	13	ns
t_{PLH}	TCKI↑	$\overline{INT}$	3.7	13.4	3.7	12.9	ns
t_{PHL}			5.5	13.5	5.5	13.1	
t_{PHL}	TCKI↑	$\overline{RDY}$	4.4	14	4.4	13.4	ns
t_{PLH}	TCKI↑	TCKO	3.3	14.8	3.3	14.1	ns
t_{PLH}	TCKI↓	TCKO	2.3	16.5	2.3	15.9	ns
t_{PHL}			3.6	16.1	3.6	15.6	
t_{PLH}	TCKI↓	TDO	2.9	18	2.9	17.5	ns
t_{PHL}			5.2	18.3	5.2	17.9	
t_{PLH}	TCKI↓	TMS	3.1	18.1	3.1	17.5	ns
t_{PHL}			5.1	18.9	5.1	18.2	
t_{PLH}	TCKI↓	TMS/EVENT	1.5	17.9	1.5	17.5	ns
t_{PHL}			3.5	19.2	3.5	18.9	
t_{PZH}	$\overline{RD}\downarrow$	DATA	3.8	18.6	3.8	17.6	ns
t_{PZL}			6.8	23.8	6.8	22.6	
t_{PZH}	TCKI↑	$\overline{INT}$	4.9	16	4.9	15.3	ns
		$\overline{RDY}$	3.6	15.9	3.6	15.3	
t_{PZH}	TCKI↓	TCKO	4.1	20	4.1	19.2	ns
t_{PZL}			4.8	18.1	4.8	17.4	
t_{PZH}	TCKI↓	TDO	4.3	20.1	4.3	19.5	ns
t_{PZL}			5	18.2	5	17.7	
t_{PZH}	TCKI↓	TMS	4.6	20.7	4.6	19.9	ns
t_{PZL}			5.1	19.4	5.1	18.5	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8990		SN74ACT8990		UNIT
			MIN	MAX	MIN	MAX	
t_{PZH}	TCKI↓	TMS/EVENT	2	19.1	2	18.8	ns
t_{PZL}			3.2	19.1	3.2	18.7	
t_{PZH}	TOFF↑	TCKO	4.6	12.4	4.6	12.2	ns
t_{PZL}			3.1	10.6	3.1	10.3	
t_{PZH}	TOFF↑	TDO	4.4	12.5	4.4	12.2	ns
t_{PZL}			3.5	11	3.5	10.8	
t_{PZH}	TOFF↑	TMS	3.1	16.2	3.1	14.7	ns
t_{PZL}			1.9	16.7	1.9	13.6	
t_{PZH}	TOFF↑	TMS/EVENT	2.3	15.3	2.3	13.8	ns
t_{PZL}			2.7	16.4	2.7	13.9	
t_{PHZ}	RD↑	DATA	3.8	18.4	3.8	15.4	ns
t_{PLZ}			4.1	17.1	4.1	14.8	
t_{PHZ}	TCKI↓	TCKO	6.7	20.4	6.7	19.8	ns
t_{PLZ}			4.8	21.1	4.8	20.4	
t_{PHZ}	TCKI↓	TDO	5.1	21.7	5.1	21.3	ns
t_{PLZ}			5	20.7	5	20.3	
t_{PHZ}	TCKI↓	TMS	6.9	22.4	6.9	21.9	ns
t_{PLZ}			4.6	20.6	4.6	20.1	
t_{PHZ}	TCKI↓	TMS/EVENT	4.7	22.5	4.7	22.1	ns
t_{PLZ}			2.8	20.5	2.8	20.1	
t_{PHZ}	TOFF↓	TCKO	5	15.6	5	15.4	ns
t_{PLZ}			4.4	15.5	4.4	15.3	
t_{PHZ}	TOFF↓	TDO	5.6	16.6	5.6	16.5	ns
t_{PLZ}			4.6	15.4	4.6	15.4	
t_{PHZ}	TOFF↓	TMS	4.8	19.1	4.8	17.1	ns
t_{PLZ}			4.4	17	4.4	15.8	
t_{PHZ}	TOFF↓	TMS/EVENT	4.5	18.8	4.5	17.3	ns
t_{PLZ}			2.4	17.1	2.4	16.2	
t_{PHZ}	TRST↓	DATA	5.7	20.9	5.7	20.8	ns
t_{PLZ}			4.2	20.3	4.2	20	
t_{PHZ}	TRST↓	$\overline{\text{INT}}$	8	19.6	8	19.5	ns
t_{PLZ}			6.1	18	6.1	17.8	
t_{PHZ}	TRST↓	$\overline{\text{RDY}}$	6.5	18.8	6.5	18.7	ns
t_{PLZ}			4.8	17.8	4.8	17.8	
t_{PHZ}	TRST↓	TMS/EVENT	6	21.1	6	21.1	ns
t_{PLZ}			4.2	20	4.2	19.9	

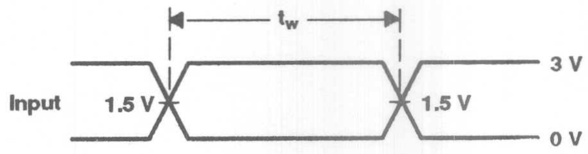
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

PARAMETER MEASUREMENT INFORMATION

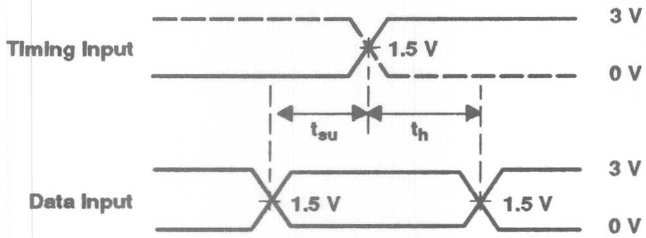


LOAD CIRCUIT FOR OUTPUTS

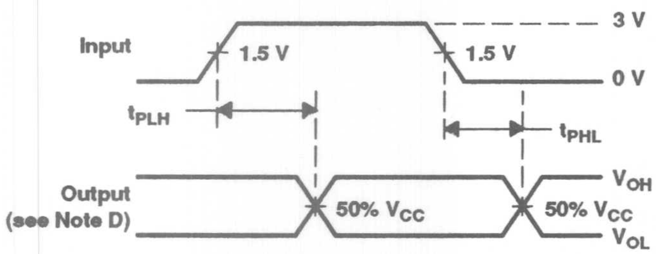
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



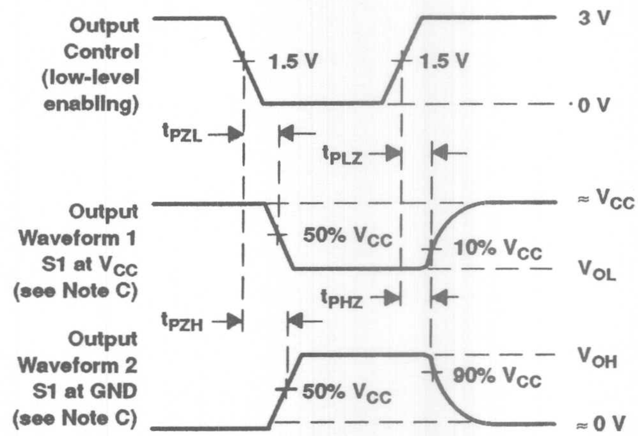
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



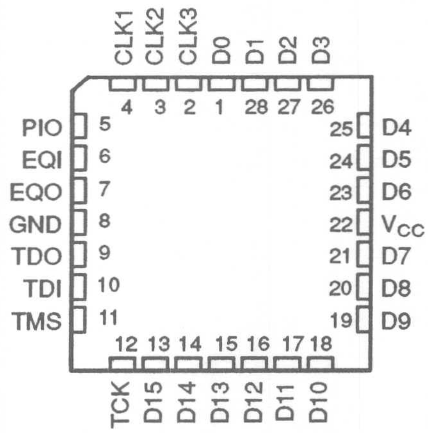
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Each Contain a 1024-Word by 16-Bit Random-Access Memory (RAM) to Store the States of a Digital Bus
- Test Operations Are Synchronous to the Test Clock or System Clock(s)
- Each Contain Texas Instruments Event Qualification Module for Real-Time System Test
- Eight Protocols for On-Line Signal Monitoring and Test Operations
- Perform Parallel Signature Analysis (PSA) of Data Inputs With User-Definable Feedback
- Data Inputs Are Maskable During PSA Operations
- Cascaded PSA Mode Allows Compression of Parallel Data Paths Greater Than 16 Bits in Width
- Direct Memory Access (DMA) Speeds Memory and Register File Read/Write Operations
- Power-Down Mode When RAM Is Idling Reduces Power Dissipation
- Compatible With Texas Instruments *ASSET*™ (Advanced Support System for Emulation and Test) Software
- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Packaged in 28-Pin Plastic and Ceramic Chip Carriers

SN54ACT8994 . . . FK PACKAGE
SN74ACT8994 . . . FN PACKAGE
(TOP VIEW)



description

The SN54ACT8994 and SN74ACT8994 digital bus monitors (DBM) are members of the Texas Instruments SCOPE™ testability IC family. This family of components supports IEEE Standard 1149.1-1990 (JTAG) boundary scan to facilitate testing of complex circuit board assemblies. The DBM is a boundary-scannable device designed to monitor and/or store the values of a digital bus up to sixteen bits in width. It resides in parallel with the bus being monitored.

Data at the D-input pins can be stored in a scannable random-access memory (RAM). Up to 1024 words of 16 bits can be stored. A parallel signature analysis (PSA) can be performed on the data or on the contents of memory. The PSA operations use a linear feedback shift register technique to compress data into a signature. The user can configure the device to mask any combination of data inputs and control the feedback used during PSA operations.

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description (continued)

The DBM receives instructions via the IEEE-Standard-1149.1-1990 test access port (TAP) interface. The TAP interface consists of test clock (TCK), test mode select (TMS), test data input (TDI), and test data output (TDO) pins.

The DBM can be operated in the off-line mode or the on-line mode. In the off-line mode, the device can perform test operations independent of system conditions. Off-line test operations include parallel signature analysis on the contents of RAM and external test.

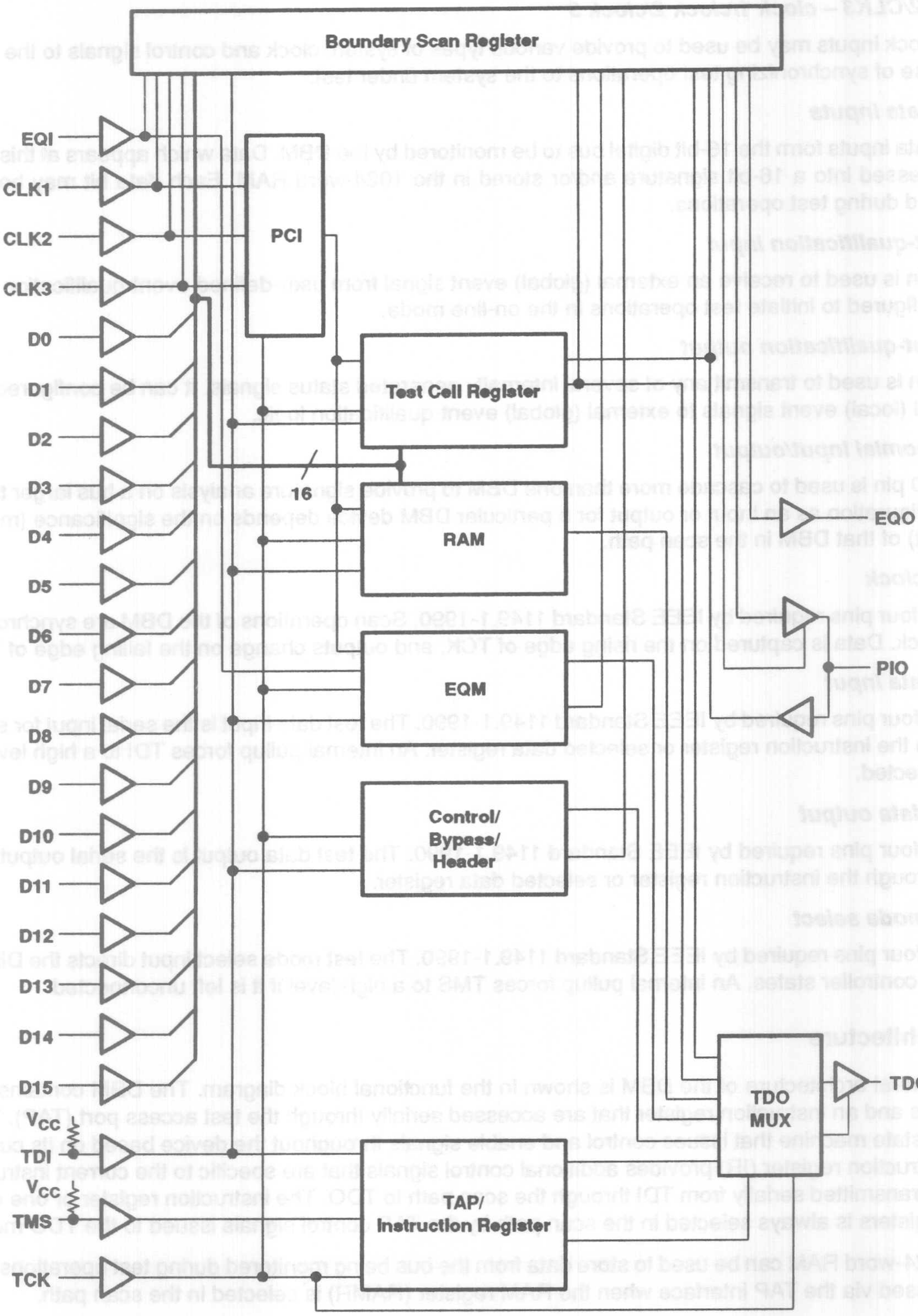
In the on-line mode, the DBM can be configured to perform test operations that are initiated based on system conditions and that operate synchronously to a logical combination of one or more system clocks. The device allows sample, storage, and/or PSA operations to be performed according to one of eight protocols. Compare patterns, which can be stored in the event-qualification module (EQM), allow the user to define specific values of the 16-bit bus for which the test operations are to be performed.

The 1024-word by 16-bit RAM and the EQM register files can be serially accessed using IEEE-Standard-1149.1-1990-compatible read and write instructions. However, direct memory access (DMA) instructions are also provided to speed transfer of large amounts of data to and from the RAM and EQM.

The polynomial input/output (PIO) is a bidirectional pin used to cascade more than one DBM to provide signature analysis on a bus larger than 16 bits.

The SN54ACT8994 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT8994 is characterized for operation from 0°C to 70°C.

functional block diagram



terminal descriptions

CLK1/CLK2/CLK3 – clock 1/clock 2/clock 3

The clock inputs may be used to provide various types of system clock and control signals to the DBM for the purpose of synchronizing test operations to the system under test.

D15-D0 – data inputs

The data inputs form the 16-bit digital bus to be monitored by the DBM. Data which appears at this bus may be compressed into a 16-bit signature and/or stored in the 1024-word RAM. Each data bit may be individually masked during test operations.

EQI – event-qualification input

This pin is used to receive an external (global) event signal from user-defined event-qualification logic. It can be configured to initiate test operations in the on-line mode.

EQO – event-qualification output

This pin is used to transmit any of several internally generated status signals. It can be configured to transmit internal (local) event signals to external (global) event-qualification logic.

PIO – polynomial input/output

This I/O pin is used to cascade more than one DBM to provide signature analysis on a bus larger than 16 bits. Its configuration as an input or output for a particular DBM device depends on the significance (most, middle, or least) of that DBM in the scan path.

TCK – test clock

One of four pins required by IEEE Standard 1149.1-1990. Scan operations of the DBM are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.

TDI – test data input

One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if it is left unconnected.

TDO – test data output

One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.

TMS – test mode select

One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the DBM through its TAP controller states. An internal pullup forces TMS to a high level if it is left unconnected.

general architecture

The general architecture of the DBM is shown in the functional block diagram. The DBM contains eight data registers and an instruction register that are accessed serially through the test access port (TAP). The TAP is a finite-state machine that issues control and enable signals throughout the device based on its current state. The instruction register (IR) provides additional control signals that are specific to the current instruction. Test data is transmitted serially from TDI through the scan path to TDO. The instruction register or one of the eight data registers is always selected in the scan path by the TAP control signals issued to the TDO multiplexer.

The 1024-word RAM can be used to store data from the bus being monitored during test operations. The RAM is accessed via the TAP interface when the RAM register (RAMR) is selected in the scan path.

general architecture (continued)

The event-qualification module (EQM) contains two data registers that contain configuration, compare, and mask data associated with on-line test operations. The EQM also contains the state machines for the eight protocols that include various start/stop, start/pause/resume, and do-while algorithms. These protocols operate synchronously to the clock signal generated by the programmable clock interface (PCI).

The PCI generates a clock signal from one of 32 different logical combinations of CLK1, CLK2, CLK3, and TCK. The user configures the PCI through the control register (CTLR).

The test cell register (TCR) is a data register that can perform PSA operations on the data bus or on the contents of RAM. During PSA operations, the TCR is a linear feedback shift register. The CTLR configures the data masking and controls the feedback for PSA operations.

The boundary scan register (BSR), header register (HR), and bypass register (BR) are all data registers that can be serially accessed through the TAP interface.

instruction register

The eight-bit instruction register (IR) contains the DBM's current instruction, which controls all operations of the device. When the IR is placed in the scan path, the IR status word is loaded into the IR and shifted out on TDO when the new instruction is shifted in.

The IR status word contains four status bits. The $\overline{\text{IRERR}}$ status bit is asserted when an opcode that does not exhibit even parity is loaded into the instruction register. The OVF status bit is set when the RAM address counter is incremented past its maximum value of 3FFh (register value given in hexadecimal format, indicated by the letter h following the value). The RUNINT and EOT status bits pertain to on-line testing and are set when a protocol is interrupted (RUNINT) or the end of the protocol is reached (EOT).

boundary scan register

The boundary scan register (BSR) is a 24-bit register that includes one boundary scan cell (BSC) for each of the non-JTAG input and output pins of the device, two BSCs for PIO (one for input data and one for output data), and one BSC for the PIO direction signal. The BSR is used to capture the data appearing at the device periphery and to apply test data to the device outputs.

bypass register

The bypass register (BR) is a one-bit register required by IEEE Standard 1149.1-1990. It is included to provide an abbreviated scan path through the DBM when the current test operations do not require it to access one of the other data registers.

control register

The 45-bit control register (CTLR) issues configuration, control, and enable signals to the device. Data shifted into the CTLR configures the data mask and feedback for PSA operations. It also configures the programmable clock interface and selects the test operations to be performed (see test operations).

event-qualification register 1

Event-qualification register 1 (EQR1) is a 32-bit register that configures the DBM for on-line testing (event-qualified testing). Data shifted into EQR1 selects and controls one of eight event-qualification protocols and configures the event and status signals. The event signal is used to trigger test operations according to the protocol being executed. The status signal is output via EQO. EQR1 also contains the loop counter, which controls the number of times an event-qualification protocol is executed.

event-qualification register 2

Event-qualification register 2 (EQR2) is used to load the event counter, expected data, and mask data (16-word-deep register files) for event-qualified tests. Depending on the current instruction, it is either 48 or 56 bits in length and can be thought of as three 16-bit data segments and two 4-bit address segments. One 4-bit address segment addresses the event counter, while the other 4-bit address segment addresses the expected data and mask data.

The register files can be accessed using IEEE-Standard-1149.1-1990-compatible instructions or direct memory access (DMA) instructions. When using IEEE-Standard-1149.1-1990-compatible instructions, EQR2 is configured as a 56-bit register. The data appearing in the 16-bit data segments is loaded into or out of the addresses specified by the register's two 4-bit address segments.

During execution of the DMA instructions, EQR2 is configured as a 48-bit register containing only the three 16-bit data segments. Using DMA instructions allows a continuous stream of data to be loaded or unloaded from the register files. After each 48th bit of the data stream has been shifted to or from the register files, the register file addresses are automatically incremented, and the first data bit of the next address is shifted.

header register

The header register (HR) is an 8-bit register used to initiate DMA write operations on the RAM and on the EQR2 register files. When a DMA write instruction is active, the data being shifted from TDI to TDO is compared against the current value of the HR, and the DMA write operation begins after a match is found. When the value of the HR is set to 00h, DMA write operations can only be initiated by the TAP and are not initiated by the TDI-to-TDO data flow.

random-access memory register

The random-access memory register (RAMR) is used to access the 1024-word RAM. Depending on the current instruction, it is either 16 bits or 26 bits in length and can be thought of as a 16-bit data segment and a 10-bit address segment.

The RAMR can be accessed using IEEE-Standard-1149.1-1990-compatible instructions or direct memory access (DMA) instructions. When using the IEEE-Standard-1149.1-1990-compatible instructions, RAMR is configured as a 26-bit register. The data appearing in the 16-bit data segment is loaded into or out of the address specified by the register's 10-bit address.

During execution of the DMA instructions, RAMR is configured as a 16-bit register containing only the 16-bit data segment. Using DMA instructions allows a continuous stream of data to be loaded or unloaded from the register. After each 16th bit of the data stream has been shifted to or from the register, the address is automatically incremented, and the first data bit of the next address is shifted.

test cell register

The test cell register (TCR) is a 16-bit register. It can perform parallel signature analysis operations on the data inputs or on the contents of RAM. The resulting signature can be scanned out and compared against an expected value. The TCR is also used during test operations to capture the current value of the data bus.

test operations

The primary function of the DBM is to perform test operations while monitoring a digital bus. The test operations can be initiated by system conditions (on-line mode) or independent of system conditions (off-line mode). The following is a description of each of the system test operations.

sample

The data at the D inputs is captured in the test cell register and can be shifted out via TDO for inspection.

parallel signature analysis

A parallel signature analysis (PSA) is performed on the data appearing at the D inputs. The test cell register is configured as a linear feedback shift register that compresses the data into a signature. The user can configure the device to mask data bits from PSA operations and control the feedback of the linear feedback shift register. When an input is masked, it is ignored and has no effect on the generated signature.

trace

The data at the D inputs is stored in the RAM. The RAM address is automatically incremented after each write cycle. The device can be configured to clear the RAM address to 000h at the beginning of test execution. It can also be configured to allow write cycles to continue after the maximum address 3FFh is reached (thus clearing the address to 000h and overwriting data).

trace/PSA

The trace and PSA operations are executed simultaneously. All the configuration options for the trace and PSA operations are available for trace/PSA.

In the off-line mode, system test operations are performed via the TAP controller. This is done independent of system conditions.

In the on-line mode, the device is configured to perform system test operations that are dependent on system conditions (event-qualified testing) and synchronous to the system clock(s). Eight different event-qualification protocols offer a wide range of test schemes that control when system test operations take place.

An event can be configured as a match between expected data from the register files and data at the D inputs (local event-qualified testing). Mask data bits from the register files allow any combination of bits to be ignored when the compare takes place. The EQI pin can also be configured as an event to trigger system test operations (global event-qualified testing).

The device can be configured to output one of several different status signals via EQO. These are used for global event-qualified testing.

The DBM has instructions that enable the user to perform a self-test on the RAM. This is done by filling the RAM with known values and performing a PSA on its contents. Instructions are included to expedite the loading of the RAM with known values as well as to perform PSA on the contents of the RAM.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... 0.5 V to V_{CC}
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			SN54ACT8994		SN74ACT8994		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	EQO		−3		−4	mA
		PIO, TDO		−11		−16	
I_{OL}	Low-level output current	EQO		3		4	mA
		PIO, TDO		11		16	
T_A	Operating free-air temperature		−55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54ACT8994		SN74ACT8994		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	EQO	V_{CC} = 4.5 V,	I_{OH} = −3 mA	3.6				V
		V_{CC} = 4.5 V,	I_{OH} = −4 mA			3.7		
		V_{CC} = 5.5 V,	I_{OH} = −3 mA	4.6				
		V_{CC} = 5.5 V,	I_{OH} = −4 mA			4.7		
	PIO, TDO	V_{CC} = 4.5 V,	I_{OH} = −11 mA	3.6				
		V_{CC} = 4.5 V,	I_{OH} = −16 mA			3.7		
		V_{CC} = 5.5 V,	I_{OH} = −11 mA	4.6				
		V_{CC} = 5.5 V,	I_{OH} = −16 mA			4.7		
V_{OL}	EQO	V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 3 mA		0.5			V
		V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 4 mA				0.5	
	PIO, TDO	V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 11 mA		0.5			
		V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 16 mA				0.5	
I_I	CLK, D, EQI, TCK	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND		±1		±1	μA
	TDI, TMS	V_{CC} = 5.5 V,	$V_I = V_{CC}$		±1		±1	
	TDI, TMS	V_{CC} = 5.5 V,	V_I = GND	−0.1	−20	−0.1	−20	
I_{OZ}†	PIO, TDO	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or GND		±5		±5	μA
I_{CC}	RAM disabled	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND, I_O = 0		200		200	μA
	RAM enabled	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND, I_O = 0		200		200	mA
ΔI_{CC}		V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,		1		1	mA

† For I/O pins, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			SN54ACT8994		SN74ACT8994		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Any CLK (except during PSARAM instruction)‡	0	50	0	50	MHz
		TCK (except during PSARAM instruction)‡	0	50	0	50	
		Any CLK or TCK (during PSARAM instruction)‡	0	17	0	17	
t_w	Pulse duration	Any CLK or TCK high or low	7		7		ns
t_{su}	Setup time	TDI before TCK↑	2		2		ns
		TMS before TCK↑	4		4		
		Any D before any CLK or TCK	5		5		
		EQI before any CLK or TCK	4		4		
		PIO before any CLK or TCK	1		1		
t_h	Hold time	TDI after TCK↑	5		5		ns
		TMS after TCK↑	3		3		
		Any D after any CLK or TCK	3		3		
		EQI after any CLK or TCK	2		2		
		PIO after any CLK or TCK	5		5		
t_d	Delay time	Power up to TCK↑	100*		100		ns

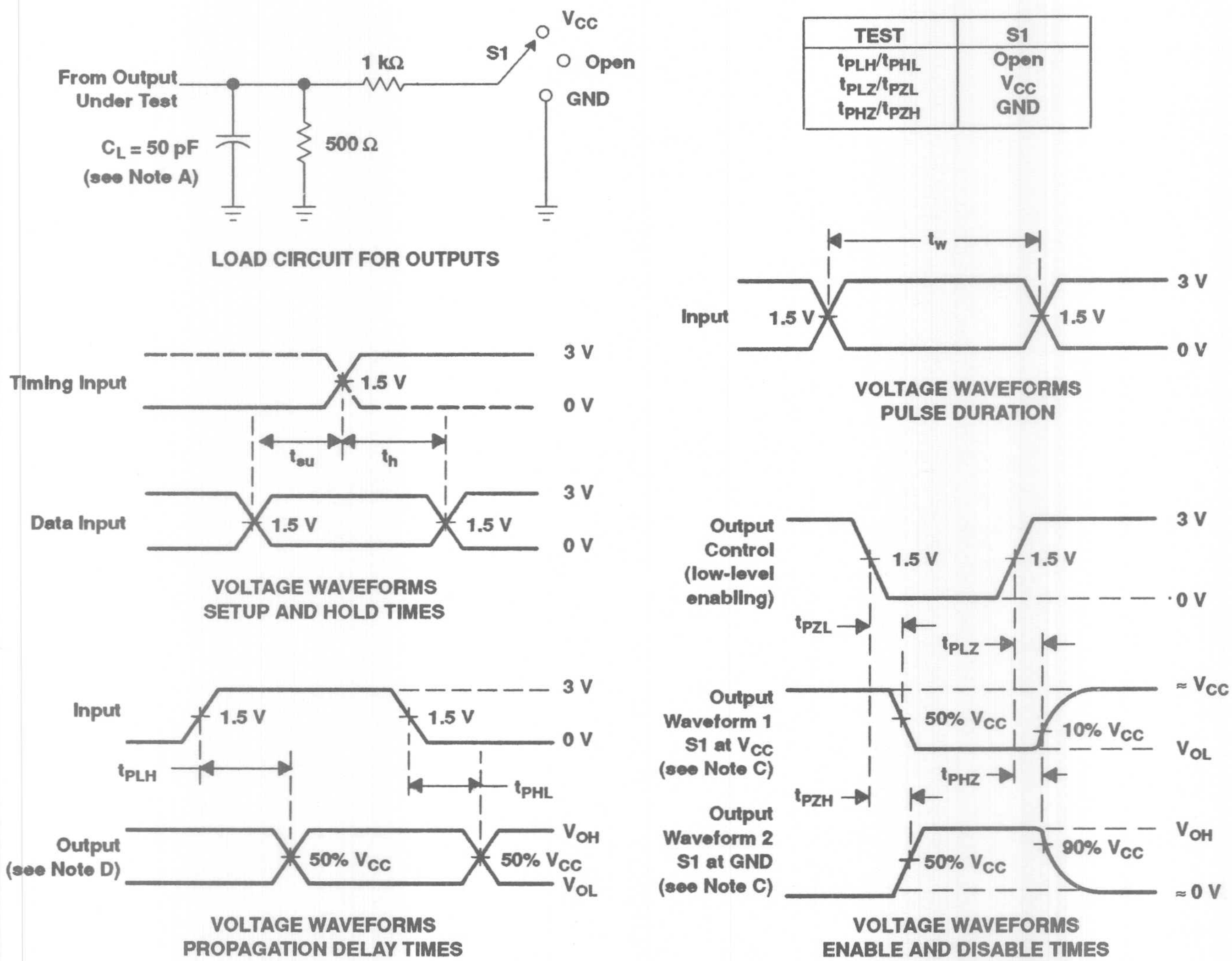
‡ The PSARAM instruction performs a parallel signature analysis on the contents of RAM. This instruction is provided to allow self-test of the RAM.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8994 MIN	SN54ACT8994 MAX	SN74ACT8994 MIN	SN74ACT8994 MAX	UNIT
f_{max}	Any CLK (except during PSARAM instruction)†		50		50		MHz
	TCK (except during PSARAM instruction)†		50		50		
	Any CLK or TCK (during PSARAM instruction)†		17		17		
t_{PLH}	Any CLK	EQO	7	20	7	18	ns
t_{PHL}			7	20	7	17	
t_{PLH}	Any CLK	PIO	9	25	9	22	ns
t_{PHL}			9	25	9	22	
t_{PLH}	Any CLK	TDO	9	28	9	20	ns
t_{PHL}			8	21	8	19	
t_{PLH}	Any D	EQO	5	20	5	17	ns
t_{PHL}			4	17	4	15	
t_{PLH}	TCK↓	EQO	5	18	5	16	ns
t_{PHL}			5	17	5	15	
t_{PLH}	TCK↓	PIO	8	23	8	19	ns
t_{PHL}			8	23	8	19	
t_{PLH}	TCK↓	TDO	3	14	3	12	ns
t_{PHL}			3	13	3	11	
t_{PZH}	TCK↓	PIO	5	21	5	18	ns
t_{PZL}			5	21	5	18	
t_{PZH}	TCK↓	TDO	3	13	3	11	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	TCK↓	PIO	6	18	6	16	ns
t_{PLZ}			5	17	5	15	
t_{PHZ}	TCK↓	TDO	9	18	9	16	ns
t_{PLZ}			8	17	8	15	

† The PSARAM instruction performs a parallel signature analysis on the contents of RAM. This instruction is provided to allow self-test of the RAM.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

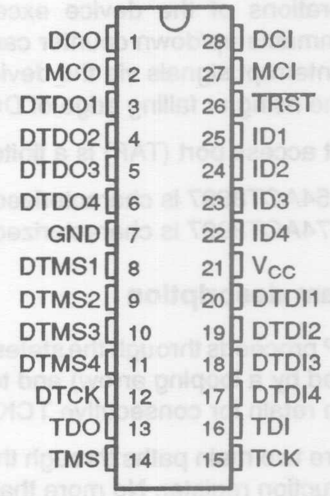
Figure 1. Load Circuit and Voltage Waveforms

SN54ACT8997, SN74ACT8997
SCAN PATH LINKERS
WITH 4-BIT IDENTIFICATION BUSES

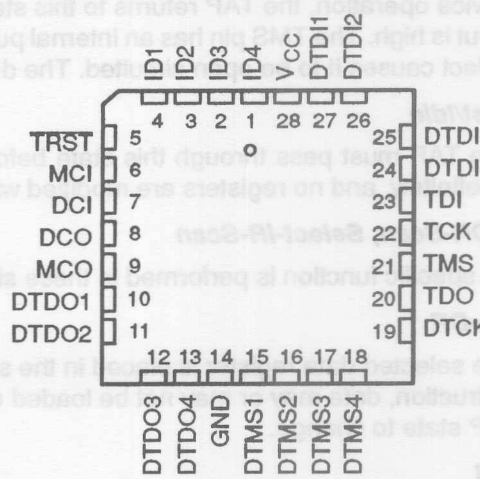
SCAS157A–D3597, APRIL 1990–REVISED AUGUST 1992

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Serial Test Bus**
- **Allow Partitioning of System Scan Paths**
- **Can Be Cascaded Horizontally or Vertically**
- **Select Up to Four Secondary Scan Paths to Be Included in a Primary Scan Path**
- **Include 8-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals**
- **Include 4-Bit Identification Bus for Scan Path Communication**
- **Compatible With TI's *ASSET*™ (Automated Support System for Emulation and Test) Software**
- **Inputs Are TTL Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic 300-mil DIPs**

SN74ACT8997 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ACT8997 . . . FK PACKAGE
(TOP VIEW)



description

The 'ACT8997 is a member of the Texas Instruments SCOPE™ testability IC family. This family of components facilitates testing of complex circuit board assemblies.

The 'ACT8997 enhances the scan capability of TI's SCOPE™ family by allowing augmentation of a system's primary scan path with secondary scan paths (SSPs), which can be individually selected by the 'ACT8997 for inclusion in the primary scan path. The device also provides buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select up to four SSPs to be included in a primary scan path. Any combination of the SSPs can be selected at a time. By selecting the bypass register, all secondary scan paths can be removed from a primary scan path.

Any of the device's six data registers or the instruction register may be placed in the device's scan path (i.e., placed between TDI (test data in) and TDO (test data out)) for subsequent shift and scan operations.

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description (continued)

All operations of the device except counting are synchronous to the test clock pin (TCK). The 8-bit programmable up/down counter can be used to count transitions on the device condition input (DCI) pin and output interrupt signals via the device condition output (DCO) pin. The device can be configured to count on either the rising or falling edge of DCI.

The test access port (TAP) is a finite-state machine compatible with IEEE Standard 1149.1.

The SN54ACT8997 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ACT8997 is characterized for operation from 0°C to 70°C.

state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

Test-Logic-Reset

In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if the test mode select (TMS) input is high. The TMS pin has an internal pullup that forces it to a high level if it is left unconnected or if a board defect causes it to be open circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states; the TAP exits either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change.

Shift-DR

In this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the logic level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the low logic level.

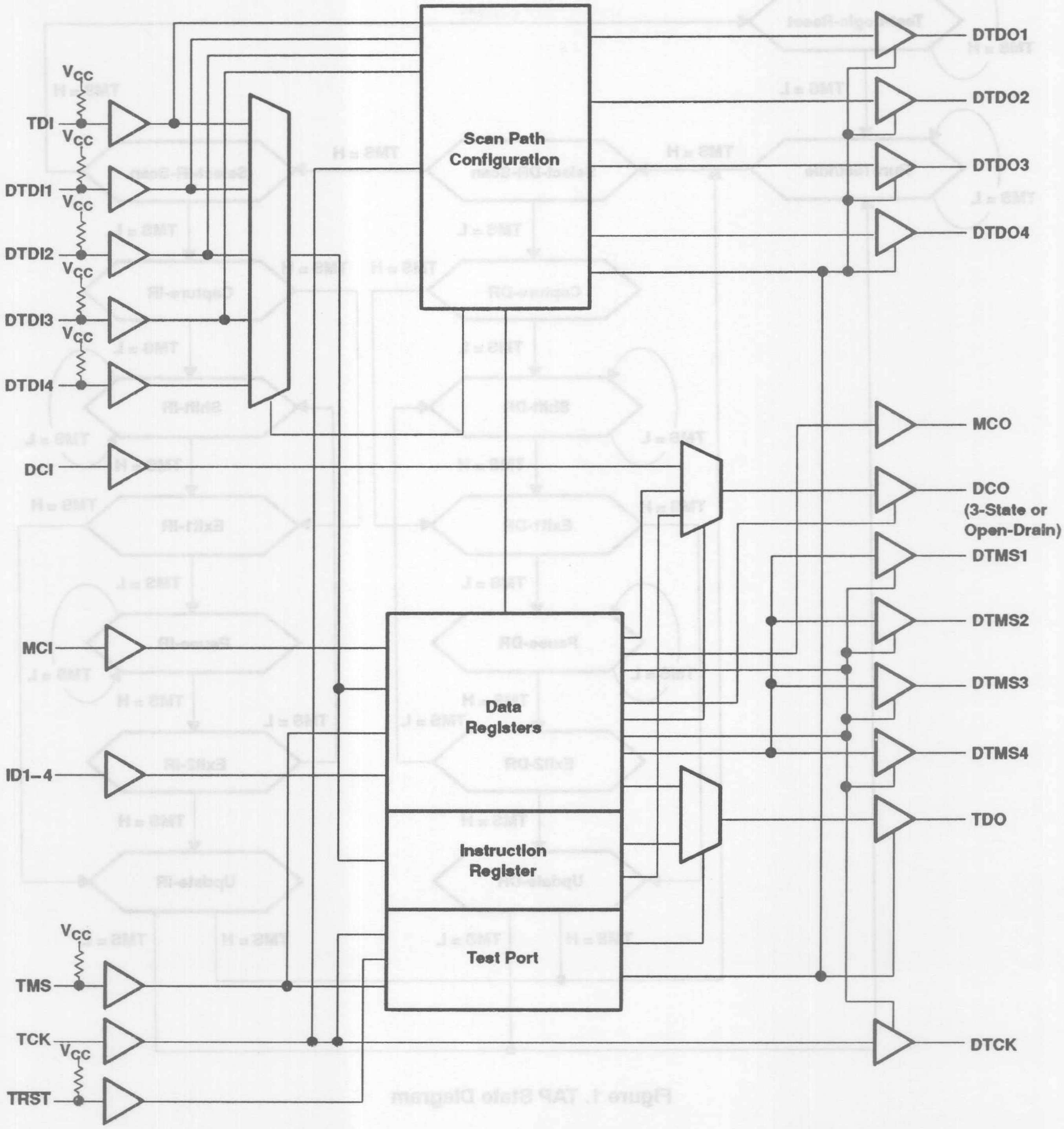
Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capatility of suspending and resuming shift operations without loss of data.

functional block diagram



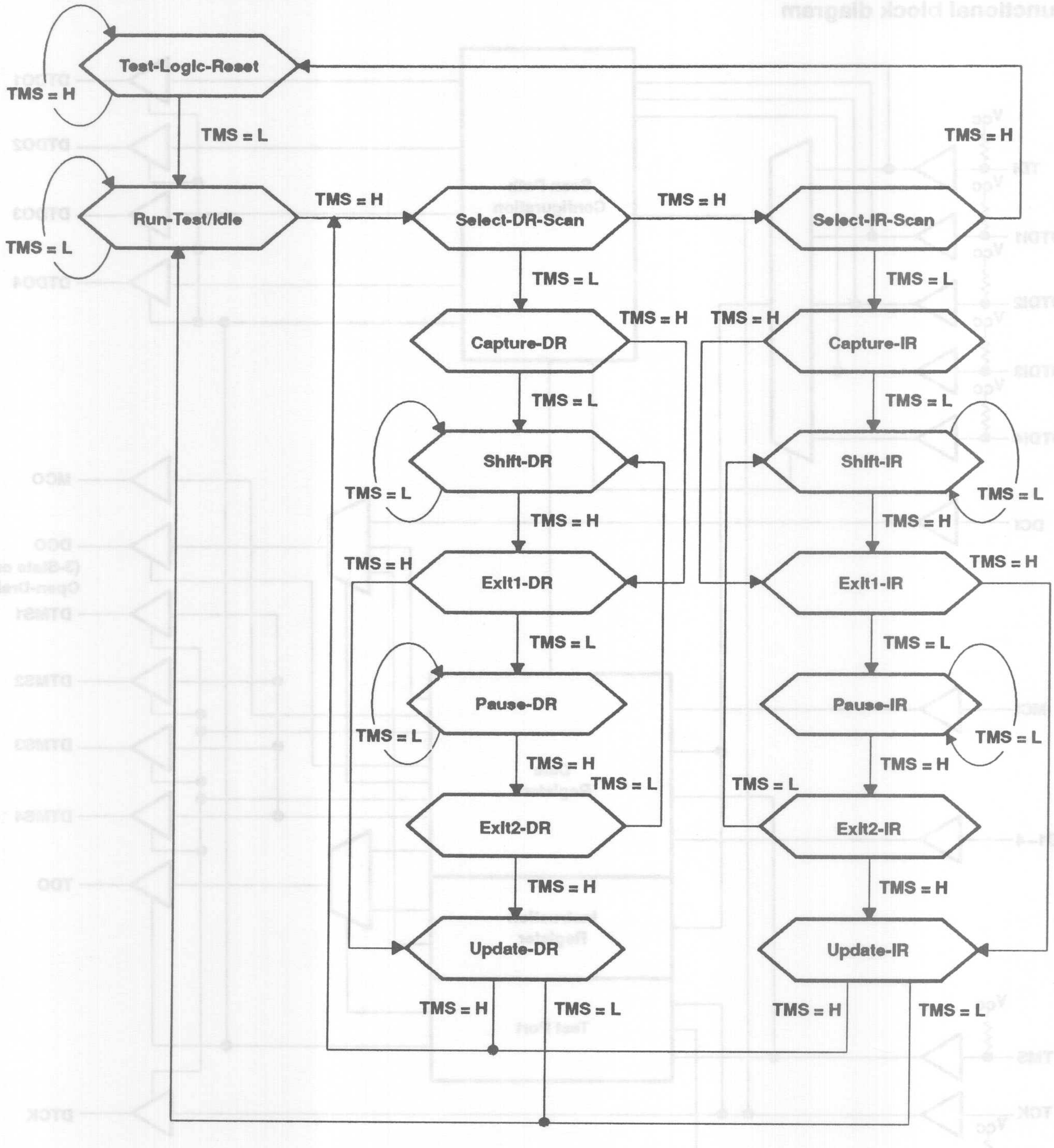


Figure 1. TAP State Diagram

state diagram description (continued)

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

Capture-IR

The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

Shift-IR

In this state, data is serially shifted through the instruction register fromTDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the high level.

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction.

signal descriptions

TDI–Test Data In

One of the four pins required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or data registers. TDI is typically driven by the TDO pin of the primary bus controller (PBC). An internal pullup forces TDI to a high level if it is left unconnected.

TDO–Test Data Out

One of the four pins required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or data registers. TDO is typically connected to the TDI pin of the next testable device in the primary scan path.

TCK–Test Clock

One of the four pins required by IEEE Standard 1149.1. All operations of the ’ACT8997, except for the count function, are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.

TMS–Test Mode Select

One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the ’ACT8997 through its states. An internal pullup forces TMS to a high level if it is left unconnected.

signal descriptions (continued)

TRST–Test Reset

This active-low pin implements the optional reset function of IEEE Standard 1149.1. When asserted, TRST causes the 'ACT8997 to go to the Test-Logic-Reset state and configure the instruction register and data registers to their power-up values. An internal pullup forces TRST to a high level if it is left unconnected.

DTMS1–DTMS4–Device Test Mode Select 1–4

Any combination of these four pins can be selected to follow the TMS pin to direct the secondary scan path(s) through the states in Figure 1. The unselected DTMS pins can be independently set to a high or low logic level. The TMS circuit monitors input from the control register to determine the configuration of the DTMS pins.

MCI–Master Condition Input

This pin receives interrupt and protocol signals from a PBC. The level on MCI is buffered and output on MCO.

MCO–Master Condition Output

This pin transmits interrupt and protocol signals to the secondary scan path(s).

DCI–Device Condition Input

This pin receives interrupt and protocol signals from the secondary scan path(s). When the counter register is instructed to count up or down, the DCI pin is configured as the counter clock.

DCO–Device Condition Output

DCO is configured by the control register to output protocol and interrupt signals and may be configured by the control register to output an error signal if the instruction register is loaded with an invalid value. DCO is further configured by the control register as:

1. Active high or active low (reset condition = active low).
2. Open drain or 3 state (reset condition = open drain).

DTDI1–DTDI4–Device Test Data In 1–4

These pins receive the serial test data outputs of the selected secondary scan path(s). An internal pullup forces DTDI1-DTDI4 to a high logic level if it is left unconnected.

DTDO1–DTDO4–Device Test Data Out 1–4

These pins output serial test data to the TDI input(s) of the secondary scan path(s).

DTCK–Device Test Clock

This pin outputs the buffered test clock TCK to the secondary scan path(s).

ID1–ID4–Identification 1–4

This 4-bit data bus can be hardwired to provide identification of the subsystem under test. The value present on the bus can be scanned out through the boundary scan or ID bus registers.

functional block description

The 'ACT8997 is intended to link secondary scan paths for inclusion in a primary scan path. Any combination of the four secondary scan paths can be linked, or the device can be bypassed entirely.

The least significant bit (LSB) of any value scanned into any register of the device is the first bit shifted in (nearest to TDO). The most significant bit (MSB) is the last bit shifted in (nearest to TDI).

The 'ACT8997 is divided into functional blocks as detailed below.

test port

The test port decodes the signals on TCK, TMS, and $\overline{TRST}$ to control the operation of the circuit. The test port includes a TAP that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP state diagram is shown in Figure 1.

instruction register

The instruction register (IR) is an 8-bit-wide serial shift register that issues commands to the device. Data is input to the instruction register via TDI (or one of the DTDI pins) and shifted out via TDO. All device operations are initiated by loading the proper instruction or set of instructions into the IR.

data registers

Six parallel data registers are included in the 'ACT8997: bypass, control, counter, boundary scan, ID bus, and select. The ID bus register is a part of the boundary scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO.

scan path configuration circuit

This circuit decodes bits in the select and control registers to determine which, if any, of the secondary scan paths are to be included in the primary scan path.

Table 1. Register Summary

REGISTER NAME	LENGTH (BITS)	FUNCTION
Instruction	8	Issue command information to the device
Control	10	Configuration and enable control
Counter	8	Count events on DCI, output interrupts via DCO
Select	8	Select one or more secondary scan paths
Boundary Scan	10	Capture and force test data at device periphery
ID Bus	4	Provide identification code
Bypass	1	Remove the 'ACT8997 from the scan path

instruction register description

The instruction register (IR) is an 8-bit serial register that outputs control signals to the device. Table 2 lists the instructions implemented in the 'ACT8997 and the data register selected by each instruction. The MSB of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal (IRERR) is generated internally as shown in Table 3. The 'ACT8997 can be configured to output IRERR via DCO if the TAP enters the Pause-IR state.

During the Capture-IR state, the IR status word is loaded. The IR status word contains information about the most recently loaded values of the instruction and select registers and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4.

Figure 2 illustrates the order of scan for the instruction register.

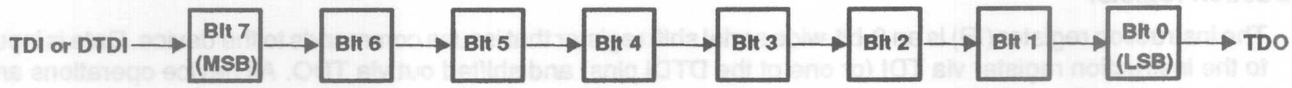


Figure 2. Instruction Register Bits and Order of Scan

Table 2. Instruction Register Opcodes

BINARY CODE BIT 7 → BIT 0 MSB → LSB	HEX VALUE	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
00000000	00	EXTEST	Boundary scan	Boundary-scan
10000001	81	BYPASS†	Bypass scan	Bypass
10000010	82	SAMPLE/PRELOAD	Sample boundary	Boundary-scan
00000011	03	INTEST	Boundary scan	Boundary-scan
10000100	84	BYPASS†	Bypass scan	Bypass
00000101	05	BYPASS†	Bypass scan	Bypass
00000110	06	BYPASS†	Bypass scan	Bypass
10000111	87	BYPASS†	Bypass scan	Bypass
10001000	88	COUNT	Count	Counter
00001001	09	COUNT	Count	Counter
00001010	0A	BYPASS†	Bypass scan	Bypass
10001011	8B	BYPASS†	Bypass scan	Bypass
00001100	0C	BYPASS†	Bypass scan	Bypass
10001101	8D	BYPASS	Bypass scan	Bypass
10001110	8E	SCANCN	Control register scan	Control
00001111	0F	SCANCT	Control register scan	Control
11111010	FA	SCANCNT	Counter scan	Counter
01111011	7B	READCNT	Counter read	Counter
11111100	FC	SCANIDB	ID bus register scan	ID bus
01111101	7D	READIDB	ID bus register read	ID bus
01111110	7E	SCANSEL	Select register scan	Select
All others		BYPASS	Bypass scan	Bypass

† A SCOPE opcode exists but is not supported by the 'ACT8997.

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instruction register description (continued)

Table 3. IRERR Function Table

# OF INSTRUCTION REGISTER BITS = 1	IRERR
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

Table 4. Instruction Register Status Word

IR BIT	VALUE‡
7	IRERR (see Table 3)
6	0
5	0
4	0
3	Level present at DCI input (1 = H, 0 = L)
2	0
1	0
0	1

‡ This value is loaded in the instruction register during the Capture-IR TAP state.

instruction register opcode description

The operation of the 'ACT8997 is dependent on the instruction loaded into the instruction register. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the Shift-DR TAP state.

All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8997.

boundary scan

This instruction implements the required EXTEST and INTEST operations of IEEE Standard 1149.1. The boundary scan register (which includes the ID bus register) is placed in the scan path. Data appearing at input pins included in the boundary scan register is captured. Data previously loaded into the output pins included in the boundary scan register is forced through the outputs.

bypass scan

This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

sample boundary

This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary scan register is placed in the scan path, and data appearing at the inputs and outputs included in the boundary scan register is sampled on the rising edge of TCK in Capture-DR.

count

The counter register begins counting on each DCI transition. The count begins from the value present in the register before the count instruction was loaded. The counter can be programmed to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while in the Run-Test/Idle TAP state.

counter register read

The counter register is placed in the scan path. During Capture-DR, the prior preloaded value of the counter is loaded into the counter register. At Update-DR, a new preload value is loaded.

counter register scan

The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, a new preload value is loaded.

control register scan

The control register is placed in the scan path for a subsequent shift operation

ID bus register scan

The ID bus register (a subset of the boundary scan register) is placed in the scan path for a subsequent shift operation. The data appearing on the ID bus is loaded into the ID bus register on the rising edge of TCK in Capture-DR.

ID bus register read

The ID bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

select register scan

The select register is placed in the scan path for a subsequent shift operation.

control register description

The control register (CTLR) is a 10-bit serial register that controls the enable and select functions of the 'ACT8997. A reset operation forces all bits to a low logic level. The contents of the control register are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5.

The enable and select functions of the control register bits are mapped as follows:

Bit 9–$\overline{\text{Up}}$/Down

This bit sets the count mode of the counter register (reset condition = count up).

Bit 8–Latch on Zero

The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 9 = 0.

Bit 7–DCO Polarity Select

DCO can be configured as an active-low or active-high output (reset condition = active low). When active low, DCO does not invert the signal selected to drive it. When active high, DCO inverts the selected signal.

Bit 6/Bit 5–DCO Source Select 1/DCO Source Select 0

DCO can be used to output the $\overline{\text{IRERR}}$ signal generated by the 'ACT8997 (see Table 3). Bits 6 and 5 can be set to output $\overline{\text{IRERR}}$ via DCO on the falling edge of TCK in the Pause-IR state. DCO can also be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

Bit 4–Parity Mask

The signal $\overline{\text{IRERR}}$ can be masked from appearing on DCO even if bits 6 and 5 are set such that it is output in the Pause-IR state (reset condition = do not mask $\overline{\text{IRERR}}$).

Table 5. Control Register Bit Mapping

BIT	VALUE	FUNCTION
9	0	Configure counter to count up
	1	Configure counter to count down
8	0	Do not stop counting when the count reaches 00000000
	1	Stop counting when the count reaches 00000000 (count down only)
7	0	Configure DCO as an active-low output
	1	Configure DCO as an active-high output
6, 5	00	DCO = H or L (depends on CTLR bit 7)
	01	DCO = $\overline{\text{IRERR}}$
	10	DCO = $\overline{\text{CE}}$, an internal logic 0 generated when the count is 00000000 (count down) or 11111111 (count up)
	11	DCO = DCI
4	0	Do not mask $\overline{\text{IRERR}}$ from DCO
	1	Mask $\overline{\text{IRERR}}$ from DCO
3	0	Configure DCO as an open-drain output
	1	Configure DCO as a 3-state output
2	0	Disable DCO
	1	Enable DCO
1	0	DCI = DCI
	1	DCI = $\overline{\text{DCI}}$ (invert the DCI signal before applying it to the internal logic)
0	0	Enable DTCK, DTDO1–4, and DTMS1–4
	1	Disable DTCK, DTDO1–4, and DTMS1–4

control register description (continued)

Bit 3–DCO Drive Select

DCO can be configured as either an open-drain or 3-state output (reset condition = open drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The 3-state configuration allows the DCO output to be connected to a bus.

Bit 2–DCO Enable

When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

Bit 1–DCI Polarity Select

The level at the DCI input can be inverted before being applied to the internal logic of the device (reset condition = do not invert DCI).

Bit 0–Device Test Pins Output Enable

DTCK, DTDO, and DTMS1–4 pins can be placed in the high-impedance state (disabled) with this bit (reset condition = enabled).

Several control register bits affect the functionality of the DCO output. The DCO function table is given in Table 6.

Figure 3 illustrates the order of scan for the control register.

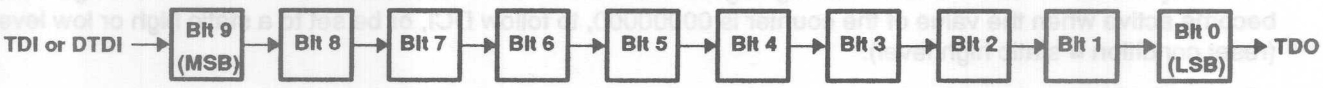

Figure 3. Control Register Bits and Order of Scan

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control register description (continued)

Table 6. DCO Function Table

DCI	INTERNAL SIGNALS†		CONTROL REGISTER BITS‡							DCO
	IRERR	CE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	
X	X	X	X	X	X	X	0	0	X	H
X	X	X	X	X	X	X	1	0	X	Z
X	X	X	0	0	0	X	X	1	X	H
X	X	X	1	0	0	X	X	1	X	L
X	X	X	0	0	1	1	X	1	X	H
X	X	X	1	0	1	1	X	1	X	L
X	0	X	0	0	1	0	X	1	X	L in Pause-IR§, H otherwise
X	1	X	0	0	1	0	X	1	X	H
X	0	X	1	0	1	0	X	1	X	H in Pause-IR§, L otherwise
X	1	X	1	0	1	0	X	1	X	L
X	X	0	0	1	0	X	X	1	X	L
X	X	0	1	1	0	X	X	1	X	H
X	X	1	0	1	0	X	X	1	X	H
X	X	1	1	1	0	X	X	1	X	L
L	X	X	0	1	1	X	X	1	0	L
L	X	X	0	1	1	X	X	1	1	H
L	X	X	1	1	1	X	X	1	0	H
L	X	X	1	1	1	X	X	1	1	L
H	X	X	0	1	1	X	X	1	0	H
H	X	X	0	1	1	X	X	1	1	L
H	X	X	1	1	1	X	X	1	0	L
H	X	X	X	1	1	1	X	X	1	H

† These signals are generated as described elsewhere in this data sheet.

‡ The control register must contain these values after the TAP has passed through its most recent Update-DR state.

§ DCO becomes active on the falling edge of TCK as the TAP enters the Pause-IR state and becomes inactive on the falling edge of TCK as the TAP enters Exit2-IR.

select register description

The select register (SR) is an 8-bit serial register that determines which, if any, of the secondary scan paths will be included in the primary scan path. A reset operation forces all bits to a logic 0.

The register is divided into four 2-bit sections, each of which controls one SSP. Figure 4 shows the mapping of the bits to the SSPs and the order of scan. For each SSP, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB of SSP2 and bit 2 is the LSB of SSP2).

When an 8-bit value is loaded into the select register, the configuration of one or more DTMS pins may change. If the new value of the SR configures a DTMS pin to a static (high or low) level, it will assume that level on the falling edge of TCK in the Update-DR TAP state. This condition is independent of any previous SR configurations. If the new value of the SR forces a DTMS pin to follow TMS (i.e., select the secondary scan path) and one or more DTMS pins are currently in the TMS follow mode, the transfer of DTMS lines will occur on the falling edge of TCK in the Update-DR TAP state. If, however, the new configuration forces a DTMS pin to follow TMS while no other DTMS pin is selected, the DTMS pin will not begin following TMS until the falling edge of TCK in the Run-Test/Idle TAP state. Therefore, when an SSP is initially selected, the TAP state should travel from Update-DR to Run-Test/Idle, not from Update-DR to Select-DR-Scan.

Although any combination of SSPs can be selected, the order of scan for each combination is fixed (see data flow description for details).

The SR bit decoding is shown in Table 7.

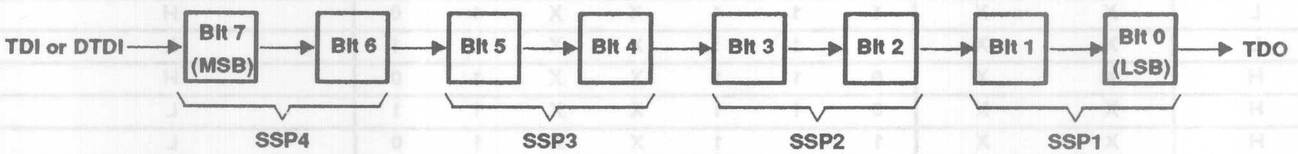


Figure 4. Select Register Bits and Order of Scan

Table 7. Select Register Bit Decoding

MSB	LSB	DTMS SOURCE	DTDO STATUS
0	0	H	Z
0	1	L	Z
1	X	TMS	Active†

† The DTDO1–4 outputs are active only in the Shift-IR and Shift-DR TAP states.

boundary scan register/ID bus register description

The boundary scan register (BSR) is a 10-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary scan cells (BSCs). Table 8 lists the device signal for each of the ten BSCs that comprise the BSR.

The four BSCs connected to the ID1–4 pins form a subset of the BSR called the ID bus register (IDBR). The IDBR can be scanned without accessing the remaining BSCs of the BSR.

Figure 5 illustrates the order of scan for the boundary scan register and ID bus register.

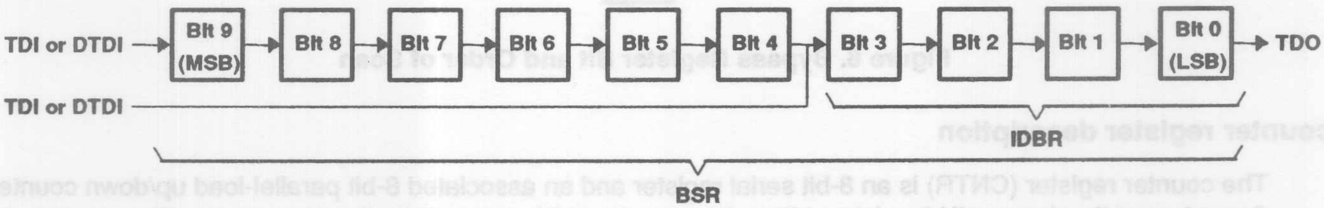


Figure 5. Boundary Scan Register Bits and Order of Scan

Table 8. Boundary Scan Register Bit Mapping

BIT	PIN NAME	SIGNAL DESCRIPTION
9	MCI	Master Condition In
8	MCO	Master Condition Out
7	DCI	Device Condition In
6	DCOTS†	Enable control for DCO in 3-state configuration (active low)
5	DCOOD†	Enable control for DCO in open-drain configuration (active low)
4	DCO	Device Condition Out
3	ID4	Identification Bus Bit 4
2	ID3	Identification Bus Bit 3
1	ID2	Identification Bus Bit 2
0	ID1	Identification Bus Bit 1

† This internal signal cannot be observed from the I/O pins of the device.

bypass register description

The bypass register (BR) is a 1-bit serial register. The function of the BR is to provide a means of effectively removing the 'ACT8997 from the primary scan path when neither it nor any of the secondary scan paths are needed for the current test operation. At power up, the BR is placed in the scan path. During Capture-DR, the BR is preloaded with a low logic level.

Figure 6 shows the order of scan for the bypass register.

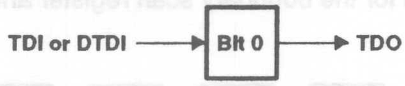


Figure 6. Bypass Register Bit and Order of Scan

counter register description

The counter register (CNTR) is an 8-bit serial register and an associated 8-bit parallel-load up/down counter. A reset operation forces all bits of the shift register to a logic 0 but does not affect the counter. The counter can be preloaded with an initial value before counting begins, and the current value of the counter scanned out via the shift register.

The counter register can be used to count events occurring on the secondary scan path(s) using the DCI pin as a counter clock and can output interrupt signals via DCO when the count has reached its end value.

An internal signal, CE, is generated as a logic 1 when the count reaches its end value (i.e., 00000000 for count down, 11111111 for count up). For any other count value, CE is a logic 0.

Many of the features of the CNTR are configured by a bit in the control register, including:

1. Count direction up or down (control register bit 9; reset condition = count up).
2. Stop counting upon counting down to 00000000 (control register bit 8; reset condition = do not latch on zero).
3. Output CE signals at DCO (control register bits 5 and 6; reset condition = output logic 0 at DCO).
4. Edge of DCI on which to trigger (control register bit 1; reset condition = positive edge).

Figure 7 shows the order of scan for the counter register.

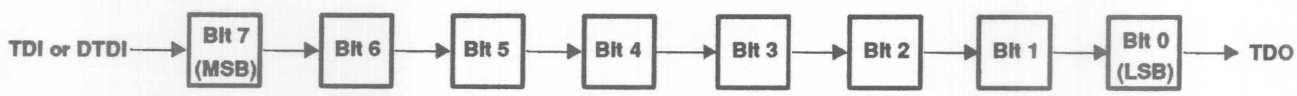


Figure 7. Counter Register Bits and Order of Scan

data flow description

The direction of serial data flow in the 'ACT8997 is dependent on the current instruction and value of the select register. Figure 8 shows the data flow when one or more SSPs have been selected. When more than one SSP has been selected, the order of scan is determined by which SSPs have been selected as shown in Table 9. Note that the 'ACT8997 adds one bit of delay from TDI or DTDI to DTDO.

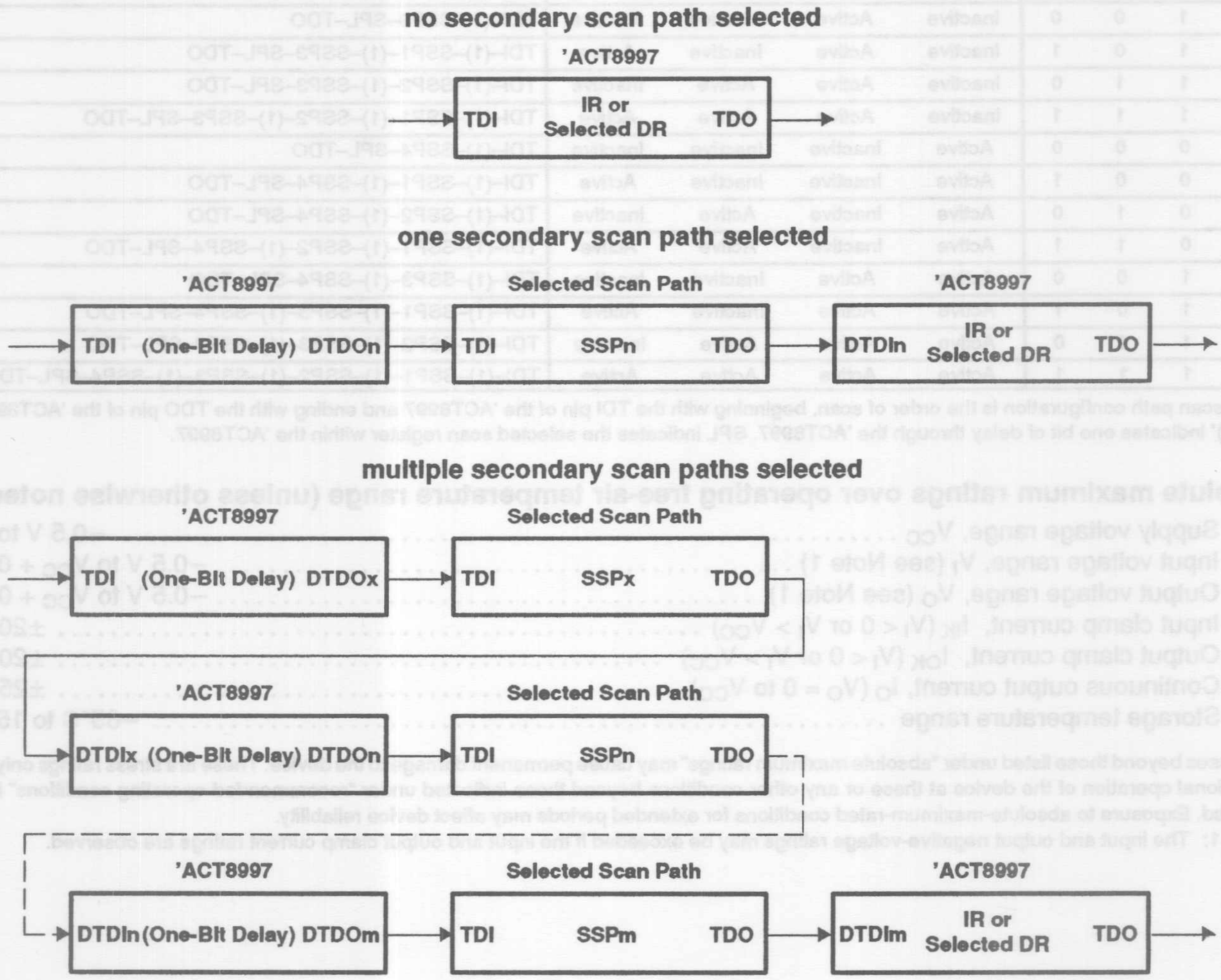


Figure 8. Data Flow in the 'ACT8997

Table 9. Scan Path Configurations

SR BIT				SSP CONFIGURATION				SCAN PATH CONFIGURATION†‡
7	5	3	1	SSP4	SSP3	SSP2	SSP1	
0	0	0	0	Inactive	Inactive	Inactive	Inactive	TDI–SPL–TDO
0	0	0	1	Inactive	Inactive	Inactive	Active	TDI–(1)–SSP1–SPL–TDO
0	0	1	0	Inactive	Inactive	Active	Inactive	TDI–(1)–SSP2–SPL–TDO
0	0	1	1	Inactive	Inactive	Active	Active	TDI–(1)–SSP1–(1)–SSP2–SPL–TDO
0	1	0	0	Inactive	Active	Inactive	Inactive	TDI–(1)–SSP3–SPL–TDO
0	1	0	1	Inactive	Active	Inactive	Active	TDI–(1)–SSP1–(1)–SSP3–SPL–TDO
0	1	1	0	Inactive	Active	Active	Inactive	TDI–(1)–SSP2–(1)–SSP3–SPL–TDO
0	1	1	1	Inactive	Active	Active	Active	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP3–SPL–TDO
1	0	0	0	Active	Inactive	Inactive	Inactive	TDI–(1)–SSP4–SPL–TDO
1	0	0	1	Active	Inactive	Inactive	Active	TDI–(1)–SSP1–(1)–SSP4–SPL–TDO
1	0	1	0	Active	Inactive	Active	Inactive	TDI–(1)–SSP2–(1)–SSP4–SPL–TDO
1	0	1	1	Active	Inactive	Active	Active	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP4–SPL–TDO
1	1	0	0	Active	Active	Inactive	Inactive	TDI–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	0	1	Active	Active	Inactive	Active	TDI–(1)–SSP1–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	1	0	Active	Active	Active	Inactive	TDI–(1)–SSP2–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	1	1	Active	Active	Active	Active	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP3–(1)–SSP4–SPL–TDO

† The scan path configuration is the order of scan, beginning with the TDI pin of the 'ACT8997 and ending with the TDO pin of the 'ACT8997.
‡ A '(1)' indicates one bit of delay through the 'ACT8997. SPL indicates the selected scan register within the 'ACT8997.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Storage temperature range .... –65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.

recommended operating conditions

			SN54ACT8997		SN74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	TDO, DTDO1–4, MCO		−8.5		−10	mA
		DTMS1–4, DCO (3-state), DTCK		−13.6		−16	
I_{OL}	Low-level output current	TDO, DTDO1–4, MCO		8.5		10	mA
		DCO (open-drain or 3-state)		13.6		16	
		DTMS1–4		20.4		24	
		DTCK		40.8		48	
T_A	Operating free-air temperature		−55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54ACT8997		SN74ACT8997		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	TDO, DTDO1–4, MCO	$I_{OH} = -8.5$ mA	4.5 V	3.7				V
		$I_{OH} = -10$ mA	4.5 V			3.7		
	DTMS1–4, DCO (3-state), DTCK	$I_{OH} = -13.6$ mA	4.5 V	3.7				
		$I_{OH} = -16$ mA	4.5 V			3.7		
V_{OL}	TDO, DTDO1–4, MCO	$I_{OL} = 8.5$ mA	4.5 V		0.5			V
		$I_{OL} = 10$ mA	4.5 V				0.5	
	DCO (open-drain or 3-state)	$I_{OL} = 13.6$ mA	4.5 V		0.5			
		$I_{OL} = 16$ mA	4.5 V				0.5	
	DTMS1–4	$I_{OL} = 20.4$ mA	4.5 V		0.5			
		$I_{OL} = 24$ mA	4.5 V				0.5	
	DTCK	$I_{OL} = 40.8$ mA	4.5 V		0.5			
		$I_{OL} = 48$ mA	4.5 V				0.5	
I_{OZ}†	DTDO1–4, DTMS1–4, DCO, DTCK	$V_O = V_{CC}$ or GND	5.5 V		±10		±5	μA
I_{OH}	DCO (open-drain)	$V_O = V_{CC}$	5.5 V		20		10	μA
I_I	MCI, DCI, TCK, ID1–4	$V_I = V_{CC}$ or GND	5.5 V		±1		±1	μA
	TDI, DTDI1–4, TMS, TRST	$V_I = V_{CC}$	5.5 V		±1		±1	
		$V_I = GND$	5.5 V	−0.1	−20	−0.1	−20	
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		100		100	μA
ΔI_{CC}‡		One input at $V_I = 3.4$ V, Other inputs at V_{CC} or GND	5.5 V		1		1	mA

† For I/O pins, the parameter I_{OZ} includes the input leakage current. For the DCO pin, the parameter I_{OZ} includes the open-drain output leakage current.

‡ This is the increase in supply current for each input being driven at TTL levels rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

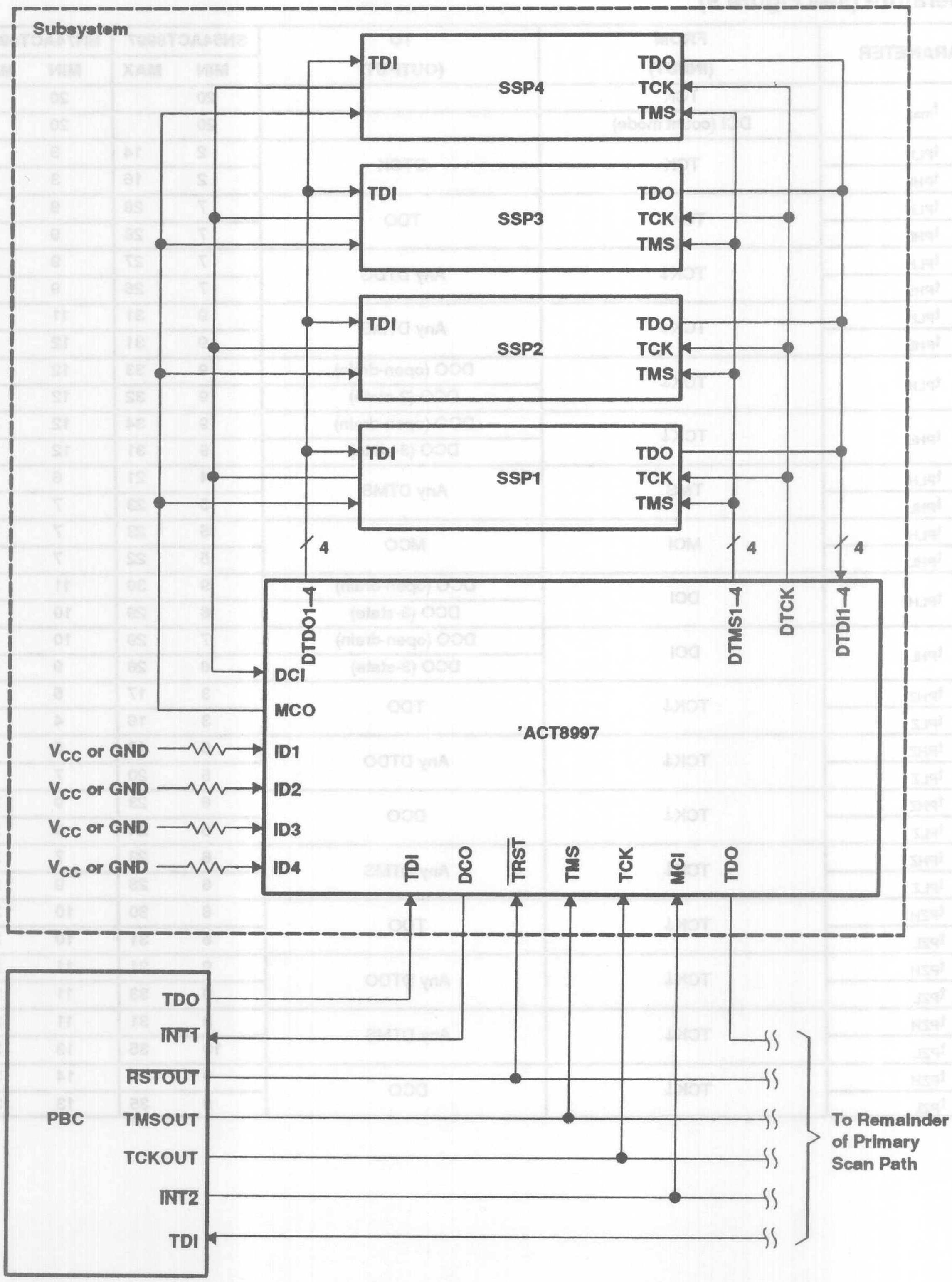
			SN54ACT8997 MIN	SN54ACT8997 MAX	SN74ACT8997 MIN	SN74ACT8997 MAX	UNIT
f_{clock}	Clock frequency	TCK	0	20	0	20	MHz
		DCI (count mode)	0	20	0	20	
t_w	Pulse duration	TCK high or low	12		12		ns
		DCI high or low (count mode)	7		7		
		$\overline{TRST}$ low	7		7		
t_{su}	Setup time	TMS before TCK↑	8		8		ns
		TDI before TCK↑	9		9		
		Any DTDI before TCK↑	7		7		
		MCI before TCK↑	3		3		
		DCI before TCK↑	3		2		
		Any ID before TCK↑	2		2		
t_h	Hold time	TMS after TCK↑	2		2		ns
		TDI after TCK↑	2		2		
		Any DTDI after TCK↑	2		2		
		MCI after TCK↑	4		4		
		DCI after TCK↑	4		4		
		Any ID after TCK↑	4		4		
t_d	Delay time	Power up to TCK↑	100*		100		ns

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

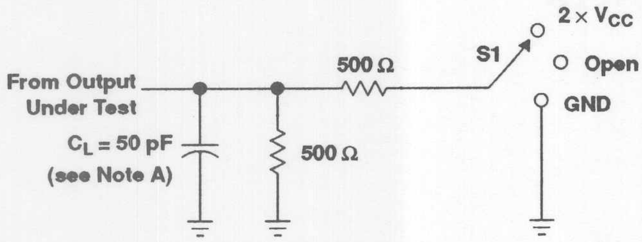
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8997		SN74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	TCK		20		20		MHz
	DCI (count mode)		20		20		
t_{PLH}	TCK	DTCK	2	14	3	12	ns
t_{PHL}			2	16	3	14	
t_{PLH}	TCK↓	TDO	7	28	9	25	ns
t_{PHL}			7	26	9	24	
t_{PLH}	TCK↓	Any DTDO	7	27	9	25	ns
t_{PHL}			7	26	9	24	
t_{PLH}	TCK↓	Any DTMS	9	31	11	29	ns
t_{PHL}			9	31	12	29	
t_{PLH}	TCK↓	DCO (open-drain)	9	33	12	31	ns
		DCO (3-state)	9	32	12	30	
t_{PHL}	TCK↓	DCO (open-drain)	9	34	12	32	ns
		DCO (3-state)	9	31	12	29	
t_{PLH}	TMS	Any DTMS	4	21	6	19	ns
t_{PHL}			5	23	7	21	
t_{PLH}	MCI	MCO	5	23	7	20	ns
t_{PHL}			5	22	7	20	
t_{PLH}	DCI	DCO (open-drain)	9	30	11	27	ns
		DCO (3-state)	6	29	10	26	
t_{PHL}	DCI	DCO (open-drain)	7	29	10	25	ns
		DCO (3-state)	6	26	9	23	
t_{PHZ}	TCK↓	TDO	3	17	5	15	ns
t_{PLZ}			3	16	4	14	
t_{PHZ}	TCK↓	Any DTDO	5	19	5	17	ns
t_{PLZ}			5	20	7	18	
t_{PHZ}	TCK↓	DCO	6	23	9	21	ns
t_{PLZ}			6	24	9	22	
t_{PHZ}	TCK↓	Any DTMS	6	23	7	21	ns
t_{PLZ}			6	28	9	26	
t_{PZH}	TCK↓	TDO	8	30	10	27	ns
t_{PZL}			8	31	10	28	
t_{PZH}	TCK↓	Any DTDO	9	31	11	28	ns
t_{PZL}			9	33	11	30	
t_{PZH}	TCK↓	Any DTMS	8	31	11	29	ns
t_{PZL}			10	35	13	33	
t_{PZH}	TCK↓	DCO	9	37	14	35	ns
t_{PZL}			8	35	13	32	

APPLICATION INFORMATION

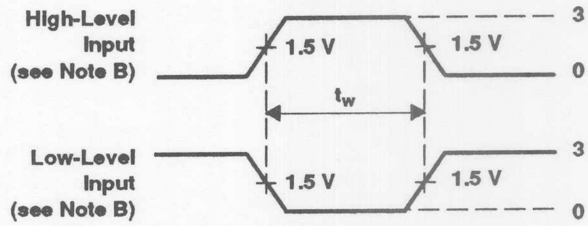


PARAMETER MEASUREMENT INFORMATION

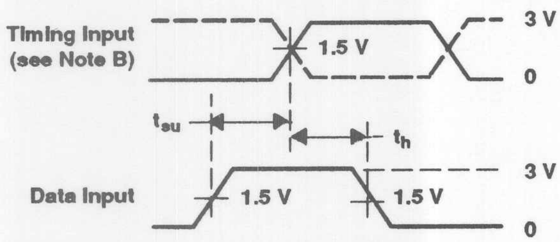


LOAD CIRCUIT FOR 3-STATE OUTPUTS

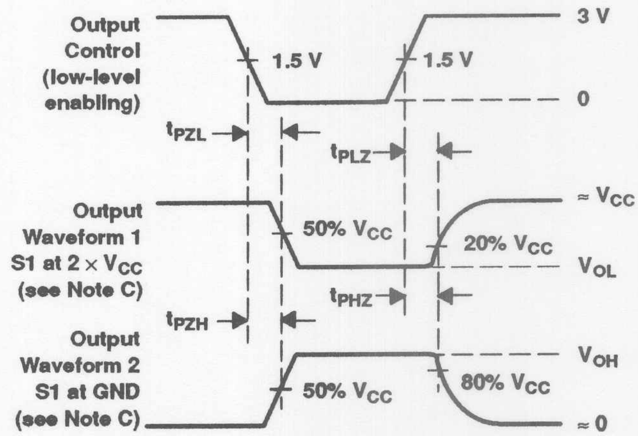
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

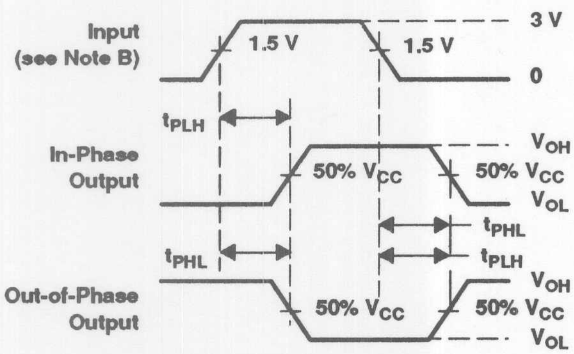


VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

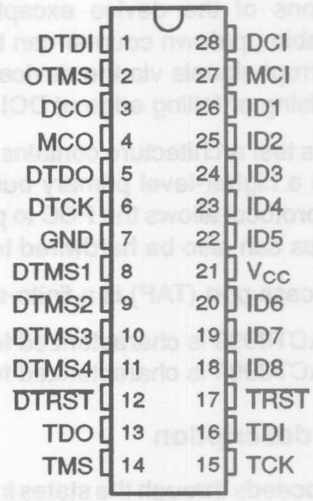
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

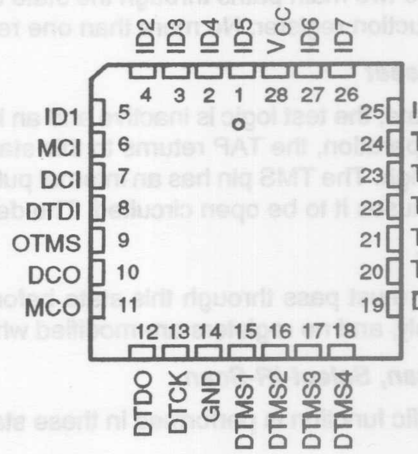
Figure 9. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Allow Partitioning of System Scan Paths**
- **Can Be Cascaded Horizontally or Vertically**
- **Select One of Four Secondary Scan Paths to Be Included in a Primary Scan Path**
- **Provide Communication Between Primary and Remote Test Bus Controllers**
- **Include 8-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals**
- **Include 8-Bit Identification Bus for Scan Path Identification**
- **Compatible With TI's *ASSET*™ (Automated Support System for Emulation and Test) Software**
- **Inputs Are TTL Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic 300-mil DIPs**

SN74ACT8999 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ACT8999 . . . FK PACKAGE
(TOP VIEW)



description

The 'ACT8999 is a member of the Texas Instruments SCOPE™ testability IC family. This family of components facilitates testing of complex circuit board assemblies.

The 'ACT8999 enhances the scan capability of TI's SCOPE™ family by allowing augmentation of a system's primary scan path with secondary scan paths (SSPs), which can be individually selected by the 'ACT8999 for inclusion in the primary scan path. The device also provides buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select one of four secondary scan paths. This has the effect of shortening the scan path to allow maximum test throughput when an individual subsystem (board or box) is to be tested. By selecting the bypass register, all secondary scan paths can be removed from a primary scan path.

Any of the device's six data registers or the instruction register may be placed in the device's scan path (i.e., placed between test data in (TDI) and test data out (TDO)) for subsequent shift and scan operations.

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description (continued)

All operations of the device except counting are synchronous to the test clock pin (TCK). The 8-bit programmable up/down counter can be used to count transitions on the device condition input (DCI) pin and output interrupt signals via the device condition output (DCO) pin. The device can be configured to count on either the rising or falling edge of DCI.

If a system's test architecture contains more than one test bus controller, the 8-bit bidirectional bus can be used to interface a higher-level primary bus controller (PBC) with one or more lower-level remote bus controllers (RBCs). A protocol allows the PBC to pass control of the 'ACT8999 to an RBC, freeing the PBC for other tasks. The 8-bit bus can also be hardwired to provide one of 256 codes for subsystem identification.

The test access port (TAP) is a finite-state machine compatible with IEEE Standard 1149.1.

The SN54ACT8999 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ACT8999 is characterized for operation from 0°C to 70°C.

state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

Test-Logic-Reset

In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if the test mode select (TMS) input is high. The TMS pin has an internal pullup that forces it to a high level if it is left unconnected or if a board defect causes it to be open circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states; the TAP exits either of them on the next TCK cycle.

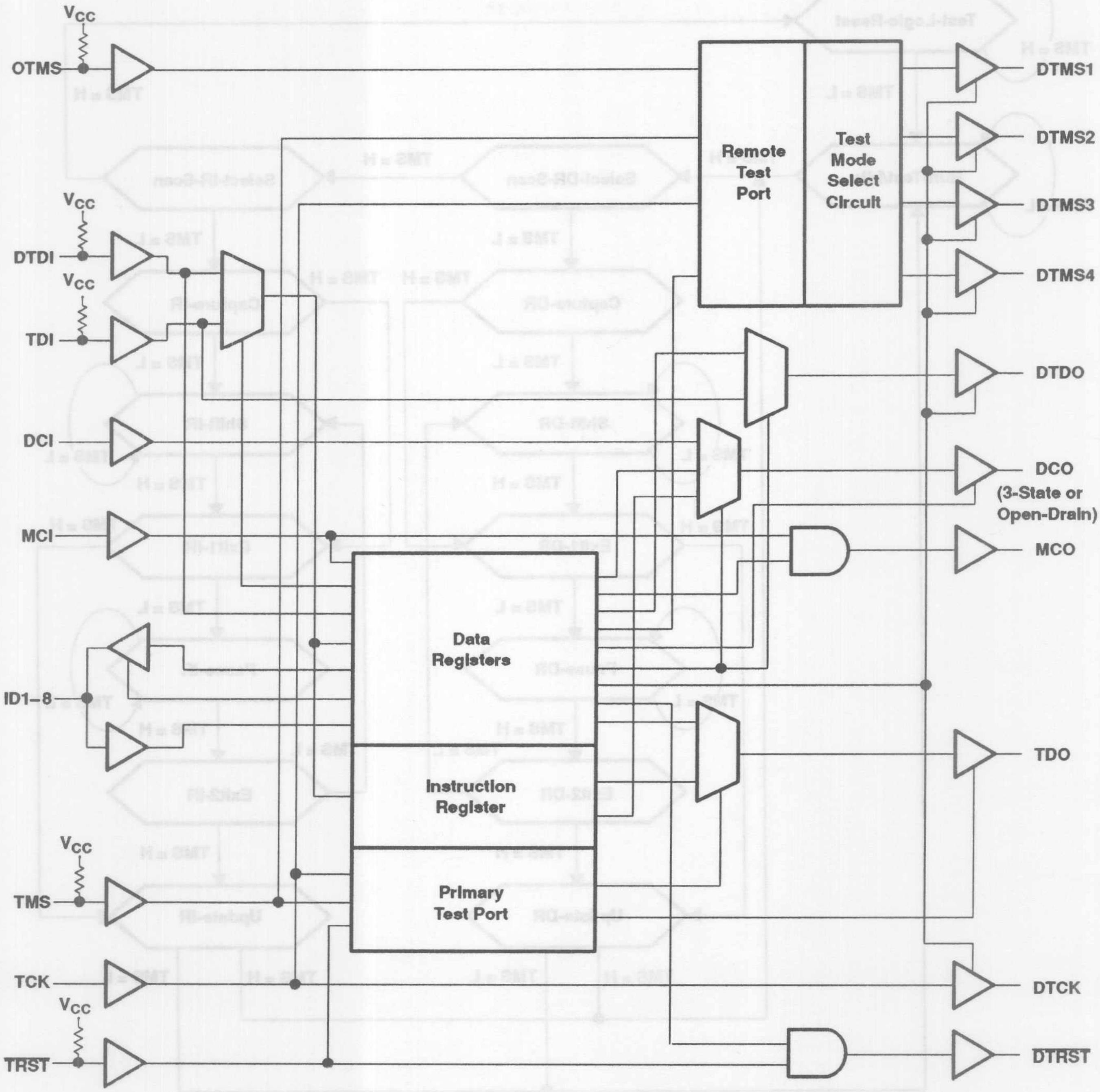
Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change.

Shift-DR

In this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the logic level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the low logic level.

functional block diagram



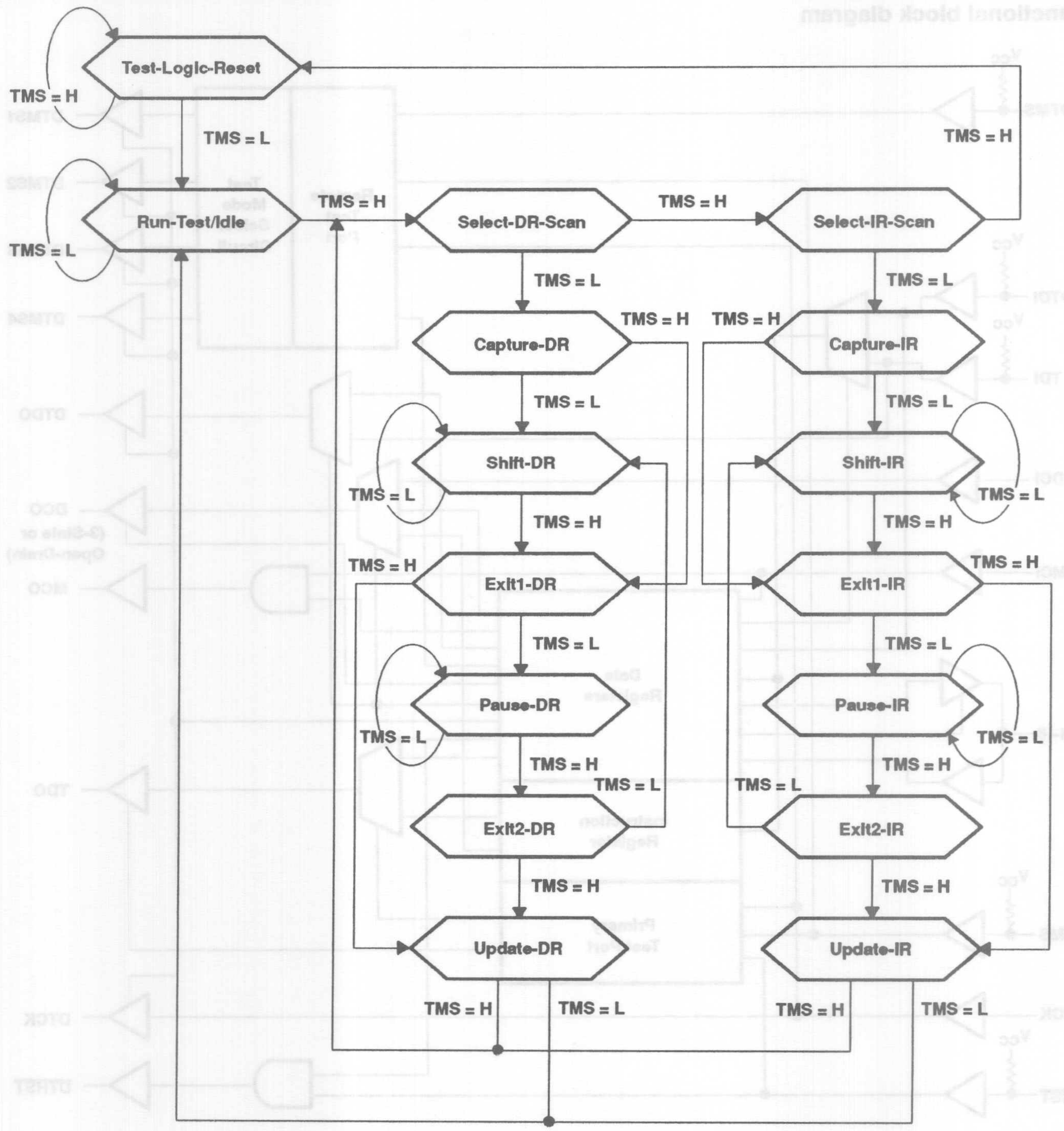


Figure 1. TAP State Diagram

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state diagram description (continued)

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capatility of suspending and resuming shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

Capture-IR

The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

Shift-IR

In this state, data is serially shifted through the instruction register fromTDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the high level.

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction.

signal descriptions

TDI–Test Data In

One of the four pins required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or data registers. TDI is typically driven by the TDO pin of the primary bus controller. An internal pullup forces TDI to a high level if it is left unconnected.

TDO–Test Data Out

One of the four pins required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or data registers. TDO is typically connected to the TDI pin of the next testable device in the primary scan path.

signal descriptions (continued)

TCK–Test Clock

One of the four pins required by IEEE Standard 1149.1. All operations of the 'ACT8999, except for the count function, are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.

TMS–Test Mode Select

One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8999 through its states. An internal pullup forces TMS to a high level if it is left unconnected.

$\overline{\text{TRST}}$–Test Reset

This active-low pin implements the optional reset function of IEEE Standard 1149.1. When asserted, $\overline{\text{TRST}}$ causes the 'ACT8999 to go to the Test-Logic-Reset state and configure the instruction register and data registers to their power-up values. $\overline{\text{TRST}}$ is also output, without inversion, via $\overline{\text{DTRST}}$ (device test reset). An internal pullup forces $\overline{\text{TRST}}$ to a high level if it is left unconnected.

OTMS–Optional Test Mode Select

This pin can be used instead of TMS to control (with TCK) the select register. This is useful when a remote bus controller is available to control the secondary scan path(s). An internal pullup forces OTMS to a high level if it is left unconnected.

DTMS1–DTMS4–Device Test Mode Select 1–4

Either none or one of these four output pins can be selected to follow the TMS pin or OTMS pin to include a secondary scan path in the primary scan path. The unselected DTMS pins can be independently set to a static high or low logic level. The TMS circuit monitors input from the control register to determine the configuration of the DTMS pins.

MCI–Master Condition Input

This pin receives interrupt and protocol signals from a PBC.

MCO–Master Condition Output

This pin transmits interrupt and protocol signals to an RBC and/or the secondary scan path(s). It also outputs an active-low error signal during the Pause-DR TAP state if an RBC loads an invalid value in the select register.

DCI–Device Condition Input

This pin receives interrupt and protocol signals from an RBC and/or the secondary scan path(s). When the counter register is instructed to count up or down, the DCI pin is configured as the counter clock.

DCO–Device Condition Output

DCO is configured by the control register to output protocol and interrupt signals to a PBC. It can also be configured by the control register to output an error signal if the instruction register or select register are loaded with invalid values. DCO is further configured by the control register as:

1. Active high or active low (reset condition = active low).
2. Open drain or 3-state (reset condition = open drain).

DTDI–Device Test Data In

This pin receives the serial test data output of the selected secondary scan path. An internal pullup forces DTDI to a high logic level if it is left unconnected.

DTDO–Device Test Data Out

This pin outputs serial test data to the TDI input(s) of the secondary scan path(s).

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signal descriptions (continued)

DTCK–Device Test Clock

This pin outputs the buffered test clock TCK to the secondary scan path(s).

DTRST–Device Test Reset

This active-low output transmits a reset signal to the secondary scan path(s). $\overline{\text{DTRST}}$ can be asserted by a bit in the control register or by setting $\overline{\text{TRST}}$ low.

ID1–ID8–Identification 1–8

This 8-bit data bus can be used to communicate with an RBC and pass data and control instructions. By wiring pullup and pulldown resistors to these pins, one of 255 unique identification codes can be assigned to the device, allowing a test controller to verify or determine the identity of the subsystem under test.

functional block description

The ’ACT8999 implements two separate functions in one package. The primary function of the device is to include a selected secondary scan path in the system’s primary scan path to enable a PBC to perform controlling and observing test functions on the selected path. This is accomplished by driving the TMS pin(s) of a secondary scan path with one of the DTMS pins of the device. This approach allows a system to have built-in testability at all levels without requiring that the primary system scan path always include all subsystem scan paths. As a result, test throughput is improved and the amount of test data that must be interpreted is reduced. The device includes error detection circuitry that prevents the user from inadvertently activating more than one secondary scan path at a time.

Another function of the device is provided by the 8-bit identification bus. This bus can be hardwired with pullup and pulldown resistors to supply an identification code to the test controller(s) to verify that test operations are being performed on the proper portion of the system. The bus can also transfer data and instructions to another device, such as a local or remote bus controller, and pass control of the scan path select function to that device. This frees the primary controller to activate another secondary scan path elsewhere in the system or perform higher-level test control functions. When the RBC is ready to return control of the device, interrupt signals alert the primary controller.

The least significant bit (LSB) of any value scanned into any register of the device is the first bit shifted in (nearest to TDO). The most significant bit (MSB) is the last bit shifted in (nearest to TDI).

The ’ACT8999 is divided into functional blocks as detailed below.

test ports

The test ports decode the signals on TCK, TMS, OTMS, and $\overline{\text{TRST}}$ to control the operation of the circuit. The test ports include a TAP that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP state diagram is shown in Figure 1.

Two test ports are included on the ’ACT8999, allowing different test controllers to command different sections of the device.

TMS circuit

The TMS circuit decodes bits in the select and control registers to determine which one, if any, of the DTMS pins (which provide mode select signals to the secondary scan path(s)) will follow the TMS pin or OTMS pin. The unselected DTMS pins are set by the circuit to a static high or low level.

instruction register

The instruction register (IR) is an 8-bit-wide serial shift register that issues commands to the device. Data is input to the instruction register via TDI or DTDI and shifted out via TDO. All device operations are initiated by loading the proper instruction or set of instructions into the IR.

functional block description (continued)

data registers

Six parallel data registers are included in the 'ACT8999: bypass, control, counter, boundary scan, ID bus, and select. The ID bus register is a part of the boundary scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO.

Table 1 summarizes the registers in the 'ACT8999.

Table 1. Register Summary

REGISTER NAME	LENGTH (BITS)	FUNCTION
Instruction	8	Issue command information to the device
Remote Instruction	8	Issue command information to the select register
Control	13	Configuration and enable control
Counter	8	Count events on DCI, output interrupts via DCO
Select	8	Select one of four DTMS pins to follow TMS or OTMS
Boundary Scan	15	Capture and force test data at device periphery
ID Bus	8	Pass test commands and data between a PBC and RBC(s)
Bypass	1	Remove the 'ACT8999 from the scan path

instruction register description

The instruction register (IR) is an 8-bit serial register that outputs control signals to the device. Table 2 lists the instructions implemented in the 'ACT8999 and the data register selected by each instruction. The MSB of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal (IRERR) is generated internally as shown in Table 3. The 'ACT8999 can be configured to output IRERR via DCO if the TAP enters the Pause-IR state.

During the Capture-IR state, the IR status word is loaded. The IR status word contains information about the most recently loaded values of the instruction and select registers and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4.

Figure 2 illustrates the order of scan for the instruction register.

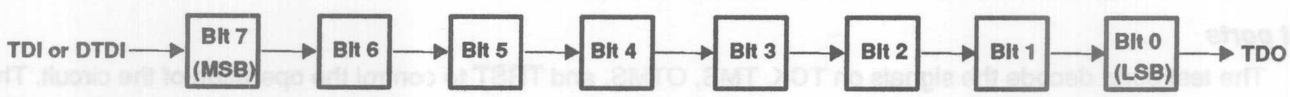

Figure 2. Instruction Register Bits and Order of Scan

instruction register description (continued)

Table 2. Instruction Register Opcodes

BINARY CODE BIT 7 → BIT 0 MSB → LSB	HEX VALUE	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
00000000	00	EXTEST	Boundary scan	Boundary-scan
10000001	81	BYPASS	Bypass scan	Bypass
10000010	82	SAMPLE/PRELOAD	Sample boundary	Boundary-scan
00000011	03	INTEST	Boundary scan	Boundary-scan
10000100	84	BYPASS†	Bypass scan	Bypass
00000101	05	BYPASS†	Bypass scan	Bypass
00000110	06	BYPASS†	Bypass scan	Bypass
10000111	87	BYPASS†	Bypass scan	Bypass
10001000	88	COUNT	Count	Counter
00001001	09	COUNT	Count	Counter
00001010	0A	BYPASS†	Bypass scan	Bypass
10001011	8B	BYPASS†	Bypass scan	Bypass
00001100	0C	BYPASS†	Bypass scan	Bypass
10001101	8D	BYPASS	Bypass scan	Bypass
10001110	8E	SCANCN	Control register scan	Control
00001111	0F	SCANCT	Control register scan	Control
11111010	FA	SCANCNT	Counter scan	Counter
01111011	7B	READCNT	Counter read	Counter
11111100	FC	SCANIDB	ID bus register scan	ID bus
01111101	7D	READIDB	ID bus register read	ID bus
01111110	7E	SCANSEL	Select register scan	Select
All others		BYPASS	Bypass scan	Bypass

† A SCOPE opcode exists but is not supported by the 'ACT8999.

Table 3. IRERR Function Table

# OF INSTRUCTION REGISTER BITS = 1	IRERR
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

Table 4. Instruction Register Status Word

IR BIT	VALUE‡
7	IRERR (see Table 3)
6	0
5	0
4	0
3	Level present at DCI input (1 = H, 0 = L)
2	SRERR (see Table 8)
1	0
0	1

‡ This value is loaded in the instruction register during the Capture-IR TAP state.

instruction register opcode description

The operation of the 'ACT8999 is dependent on the instruction loaded into the instruction register. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the Shift-DR TAP state.

All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8999.

boundary scan

This instruction implements the required EXTEST and INTEST operations of IEEE Standard 1149.1. The boundary scan register (which includes the ID bus register) is placed in the scan path. Data appearing at input pins included in the boundary scan register is captured. Data previously loaded into the output pins included in the boundary scan register is forced through the outputs.

bypass scan

This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

sample boundary

This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary scan register is placed in the scan path, and data appearing at the inputs and outputs included in the boundary scan register is sampled on the rising edge of TCK in Capture-DR.

count

The counter register begins counting on each DCI transition. The count begins from the value present in the register before the count instruction was loaded. The counter can be programmed to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while in the Run-Test/Idle TAP state.

counter register read

The counter register is placed in the scan path. During Capture-DR, the prior preloaded value of the counter is loaded into the counter register. At Update-DR, a new preload value is loaded.

counter register scan

The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, a new preload value is loaded.

control register scan

The control register is placed in the scan path for a subsequent shift operation

ID bus register scan

The ID bus register (a subset of the boundary scan register) is placed in the scan path for a subsequent shift operation. The data appearing on the ID bus is loaded into the ID bus register on the rising edge of TCK in Capture-DR.

ID bus register read

The ID bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

select register scan

The select register is placed in the scan path for a subsequent shift operation.

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control register description

The control register (CTLR) is a 13-bit serial register that controls the enable and select functions of the 'ACT8999. A reset operation forces all bits to a logic 0. The contents of the control register are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5.

The enable and select functions of the control register bits are mapped as follows:

Bit 12–$\overline{\text{Up}}$/Down

This bit sets the count mode of the counter register (reset condition = count up).

Bit 11–Latch on Zero

The counter register can be configured to stop counting when its value is 0000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 12 = 0.

Bit 10–DCO Polarity Select

DCO can be configured as an active-low or active-high output (reset condition = active low). When active low, DCO does not invert the signal selected to drive it. When active high, DCO inverts the selected signal.

Bit 9/Bit 8–DCO Source Select 1/DCO Source Select 0

DCO can be used to output two error signals generated by the 'ACT8999: $\overline{\text{IRERR}}$ (see Table 3) and $\overline{\text{SRERR}}$ (see Table 8). Bits 9 and 8 can be set to output $\overline{\text{IRERR}}$ via DCO on the falling edge of TCK in the Pause-IR state and $\overline{\text{SRERR}}$ via DCO on the falling edge of TCK in the Pause-DR state. DCO can also be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

Bit 7–Parity Mask

The internal error signals can be masked from appearing on DCO even if bits 9 and 8 are set such that $\overline{\text{IRERR}}$ and $\overline{\text{SRERR}}$ will be output in the Pause-IR and Pause-DR states (reset condition = do not mask $\overline{\text{IRERR}}$ or $\overline{\text{SRERR}}$).

Bit 6–DCO Drive Select

DCO can be configured as either an open-drain or 3-state output (reset condition = open-drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The 3-state configuration allows the DCO output to be connected to a bus.

Bit 5–DCO Enable

When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

Bit 4–DCI Polarity Select

The level at the DCI input can be inverted before being applied to the internal logic of the device (reset condition = do not invert DCI).

Bit 3–Device Test Pins Output Enable

DTCK, DTDO, and DTMS1–4 pins can be placed in the high-impedance state (disabled) with this bit (reset condition = enabled).

Bit 2–ID Bus Enable

The ID bus (ID1–8) is a bidirectional bus. The output buffers are enabled and disabled with this bit (reset condition = output buffers disabled).

control register description (continued)

Table 5. Control Register Bit Mapping

BIT	VALUE	FUNCTION
12	0	Configure counter to count up
	1	Configure counter to count down
11	0	Do not stop counting when the count reaches 00000000
	1	Stop counting when the count reaches 00000000 (count down only)
10	0	Configure DCO as an active-low output
	1	Configure DCO as an active-high output
9, 8	00	DCO = H or L (depends on CTLR bit 10)
	01	DCO = ($\overline{IRERR}$ • $\overline{SRERR}$)
	10	DCO = $\overline{CE}$, an internal logic 0 generated when the count is 00000000 (count down) or 11111111 (count up)
	11	DCO = DCI
7	0	Do not mask $\overline{IRERR}$ and $\overline{SRERR}$ from DCO
	1	Mask $\overline{IRERR}$ and $\overline{SRERR}$ from DCO
6	0	Configure DCO as an open-drain output
	1	Configure DCO as a 3-state output
5	0	Disable DCO
	1	Enable DCO
4	0	DCI = DCI
	1	DCI = $\overline{DCI}$ (invert the DCI signal before applying it to the internal logic)
3	0	Enable DTCK, DTDO, and DTMS1–4
	1	Disable DTCK, DTDO, and DTMS1–4
2	0	Disable ID1–8
	1	Enable ID1–8
1	0	Disable RBC
	1	Enable RBC
0	0	$\overline{DTRST}$ = $\overline{TRST}$
	1	$\overline{DTRST}$ = L

Bit 1–Remote Bus Controller Enable

An RBC can issue protocol and data instructions to the select register if the 'ACT8999 is configured to allow it (reset condition = RBC disabled). When an RBC is enabled, the TAP in the select register operates according to the OTMS signal.

Bit 0–Device Test Reset

$\overline{DTRST}$ can be configured to output a reset signal independently of the level on $\overline{TRST}$ (reset condition = no reset signal issued).

Several control register bits affect the functionality of the DCO output. The DCO function table is given in Table 6.

Figure 3 illustrates the order of scan for the control register.

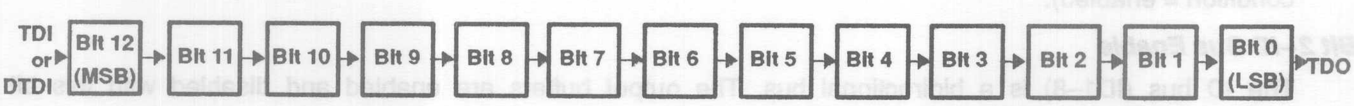

Figure 3. Control Register Bits and Order of Scan

control register description (continued)

Table 6. DCO Function Table

DCI	INTERNAL SIGNALS†			CONTROL REGISTER BITS‡							DCO
	IRERR	SRERR	CE	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	
X	X	X	X	X	X	X	X	0	0	X	H
X	X	X	X	X	X	X	X	1	0	X	Z
X	X	X	X	0	0	0	X	X	1	X	H
X	X	X	X	1	0	0	X	X	1	X	L
X	X	X	X	0	0	1	1	X	1	X	H
X	X	X	X	1	0	1	1	X	1	X	L
X	0	X	X	0	0	1	0	X	1	X	L in Pause-IR§, H otherwise
X	X	0	X	0	0	1	0	X	1	X	L in Pause-DR§, H otherwise
X	1	1	X	0	0	1	0	X	1	X	H
X	0	X	X	1	0	1	0	X	1	X	H in Pause-IR§, L otherwise
X	X	0	X	1	0	1	0	X	1	X	H in Pause-DR§, L otherwise
X	1	1	X	1	0	1	0	X	1	X	L
X	X	X	0	0	1	0	X	X	1	X	L
X	X	X	0	1	1	0	X	X	1	X	H
X	X	X	1	0	1	0	X	X	1	X	H
X	X	X	1	1	1	0	X	X	1	X	L
L	X	X	X	1	1	1	X	X	1	0	L
L	X	X	X	1	1	1	X	X	1	1	H
L	X	X	X	0	1	1	X	X	1	0	H
L	X	X	X	0	1	1	X	X	1	1	L
H	X	X	X	1	1	1	X	X	1	0	H
H	X	X	X	X	1	1	X	X	X	1	L
H	X	X	X	1	1	1	X	X	1	0	L
H	X	X	X	X	1	1	1	X	X	1	H

† These signals are generated as described elsewhere in this data sheet.

‡ The control register must contain these values after the TAP has passed through its most recent Update-DR state.

§ DCO becomes active on the falling edge of TCK as the TAP enters the appropriate pause state (Pause-IR or Pause-DR) and becomes inactive on the falling edge of TCK as the TAP enters the appropriate exit2 state (Exit2-IR or Exit2-DR).

select register description

The select register (SR) is an 8-bit serial register that determines which one, if any, of the DTMS lines follows the TMS or OTMS input. A reset operation forces all bits to a logic 0.

The register is divided into four 2-bit sections, each of which controls one DTMS output. Figure 4 shows the mapping of the bits to the DTMS outputs and the order of scan. For each DTMS pin, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB of DTMS2 and bit 2 is the LSB of DTMS2).

Only one of the four DTMS outputs can be selected to drive a secondary scan path with TMS or OTMS. If the select register is loaded with an invalid value, an error signal ($\overline{\text{SRERR}}$) is generated internally as shown in Table 8. If the TAP enters the Pause-DR state, $\overline{\text{SRERR}}$ may be output via DCO (see Table 8). If the TAP enters the Update-DR state while an invalid value is in the SR, all four DTMS outputs are set to a high level.

When a valid 8-bit value is loaded into the select register, the configuration of one or more DTMS pins may change. If the new value of the SR configures a DTMS pin to a static (high or low) level, it will assume that level on the falling edge of TCK in the Update-DR TAP state. This condition is independent of any previous SR configurations. If the new value of the SR forces a DTMS pin to follow TMS (i.e., select a single secondary scan path) and a DTMS pin is currently in the TMS/OTMS follow mode, the transfer of the DTMS line will occur on the falling edge of TCK in the Update-DR TAP state. If, however, the new configuration forces a DTMS pin to follow TMS/OTMS while no other DTMS pin is selected, the DTMS pin will not begin following TMS/OTMS until the falling edge of TCK in the Run-Test/Idle TAP state. Therefore, when an SSP is initially selected, the TAP state should travel from Update-DR to Run-Test/Idle, not from Update-DR to Select-DR-Scan.

The SR can also be accessed from an RBC. A test port in the register contains a TAP that can be enabled by the control register to monitor the values of TCK and OTMS to perform scan operations on the SR.

The SR bit decoding is shown in Table 7.

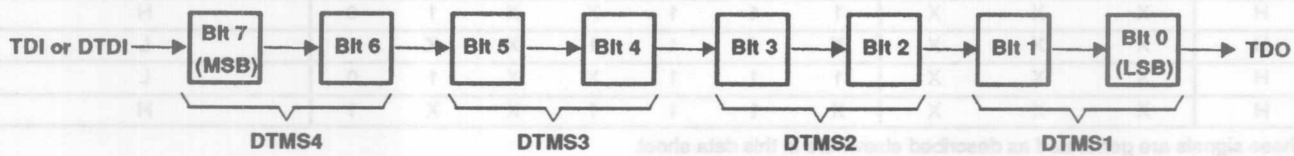

Figure 4. Select Register Bits and Order of Scan

Table 7. Select Register Bit Decoding

MSB	LSB	DTMS SOURCE
0	0	H
0	1	L
1	0	OTMS
1	1	TMS

select register description (continued)

Table 8. SRERR Function Table

SELECT REGISTER BITS								SRERR
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0	X	0	X	0	X	0	X	1
1	X	0	X	0	X	0	X	1
0	X	1	X	0	X	0	X	1
0	X	0	X	1	X	0	X	1
0	X	0	X	0	X	1	X	1
1	X	1	X	X	X	X	X	0
1	X	X	X	1	X	X	X	0
1	X	X	X	X	X	1	X	0
X	X	1	X	1	X	X	X	0
X	X	1	X	X	X	1	X	0
X	X	X	X	1	X	1	X	0

boundary scan register/ID bus register description

The boundary scan register (BSR) is a 15-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary scan cells (BSCs). Table 9 lists the device signal for each of the fifteen BSCs that comprise the BSR.

The eight BSCs connected to the ID1–8 pins form a subset of the BSR called the ID bus register (IDBR). The IDBR can be scanned without accessing the remaining BSCs of the BSR. The IDBR is used when the ID bus is enabled to allow communication between a PBC and one or more RBCs.

Figure 5 illustrates the order of scan for the boundary scan register and ID bus register.

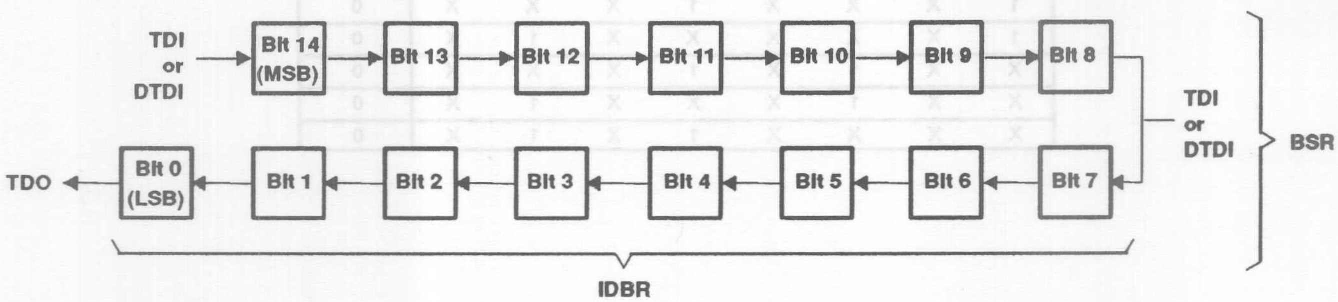

Figure 5. Boundary Scan Register Bits and Order of Scan

Table 9. Boundary Scan Register Bit Mapping

BIT	PIN NAME	SIGNAL DESCRIPTION
14	MCI	Master Condition In
13	MCO	Master Condition Out
12	DCI	Device Condition In
11	$\overline{\text{DCOTS}}$†	Enable control for DCO in 3-state configuration (active low)
10	$\overline{\text{DCOOD}}$†	Enable control for DCO in open-drain configuration (active low)
9	DCO	Device Condition Out
8	$\overline{\text{IDBOE}}$†	Enable control for ID bus (active low)
7	ID8	Identification Bus Bit 8
6	ID7	Identification Bus Bit 7
5	ID6	Identification Bus Bit 6
4	ID5	Identification Bus Bit 5
3	ID4	Identification Bus Bit 4
2	ID3	Identification Bus Bit 3
1	ID2	Identification Bus Bit 2
0	ID1	Identification Bus Bit 1

† This internal signal cannot be observed from the I/O pins of the device.

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bypass register description

The bypass register (BR) is a 1-bit serial register. The function of the BR is to provide a means of effectively removing the 'ACT8999 from the primary scan path when it is not needed for the current test operation or other function of the PBC. At power up, the BR is placed in the scan path.

Figure 6 shows the order of scan for the bypass register.

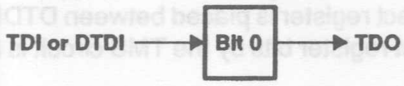


Figure 6. Bypass Register Bit and Order of Scan

counter register description

The counter register (CNTR) is an 8-bit serial register that performs a binary count if configured to do so by the control register; it uses the DCI pin as its clock. The counter can be preloaded with an initial value before counting begins, and the current value of the counter can be scanned out. The counter register can be used to count events occurring on the secondary scan path(s) and can output interrupt signals via DCO when the count has reached zero. Many of the features of the CNTR are configured by a bit in the control register, including:

1. Count direction (up or down).
2. Stop counting when the value of the register is 00000000.
3. DCI transition on which the counter counts (low-to-high or high-to-low).

An internal signal, $\overline{CE}$, is generated as a logic 0 when the value of the CNTR is 00000000. For any other value of the CNTR, $\overline{CE}$ = 1.

Figure 7 shows the order of scan for the counter register.

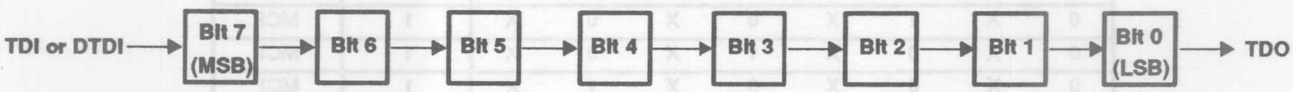


Figure 7. Counter Register Bits and Order of Scan

enabling a remote bus controller

Bit 1 in the control register allows a remote bus controller to control parts of the 'ACT8999. When an RBC is enabled, the remote test port (RTP) in the select register is activated. The remote test port operates according to the same state diagram as the primary test port but only has access to the select register. Operation of the RTP is synchronous to TCK. OTMS is the RTP's mode select pin.

The RTP contains an 8-bit instruction register. Data is shifted in via DTDI and shifted out via DTDO. As shown in Table 10, only one instruction selects something other than the bypass register to be included in the scan path. When SCANSEL is executed, the select register is placed between DTDI and DTDO. The function of the select register and the decoding of the select register bits by the TMS circuit is identical, regardless of which test port accesses the register.

An internal error signal ($\overline{\text{RSRERR}}$) is generated if an RBC loads an invalid value in the select register, and the MCO output goes low if the $\overline{\text{RSRERR}}$ is active and the remote TAP enters the Pause-DR state. The function table for $\overline{\text{RSRERR}}$ is shown in Table 11.

The RTP does not have access to the control register, so it cannot disable itself. The PBC must reset bit 1 in the control register to return control of the select register to the primary test port.

Table 10. Remote Test Port Instruction Register Opcodes

BINARY CODE BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
01111110	SCANSEL	Selected register scan	Select
All other	BYPASS	Bypass scan	Bypass

Table 11. $\overline{\text{RSRERR}}$ Function Table

SELECT REGISTER BITS								$\overline{\text{RSRERR}}$	MCO†
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
0	X	0	X	0	X	0	X	1	MCI
1	X	0	X	0	X	0	X	1	MCI
0	X	1	X	0	X	0	X	1	MCI
0	X	0	X	1	X	0	X	1	MCI
0	X	0	X	0	X	1	X	1	MCI
1	X	1	X	X	X	X	X	0	L
1	X	X	X	1	X	X	X	0	L
1	X	X	X	X	X	1	X	0	L
X	X	1	X	1	X	X	X	0	L
X	X	1	X	X	X	1	X	0	L
X	X	X	X	1	X	1	X	0	L

† This table is valid only when the remote TAP is in the Pause-DR state. Under any other condition, MCO = MCI.

data flow description

The direction of serial data flow in the 'ACT8999 is dependent on the current instruction. Figure 8 shows the data flow for the different operating modes of the device. Note that when a secondary scan path is selected, the 'ACT8999 adds one bit of delay from TDI to DTDO.

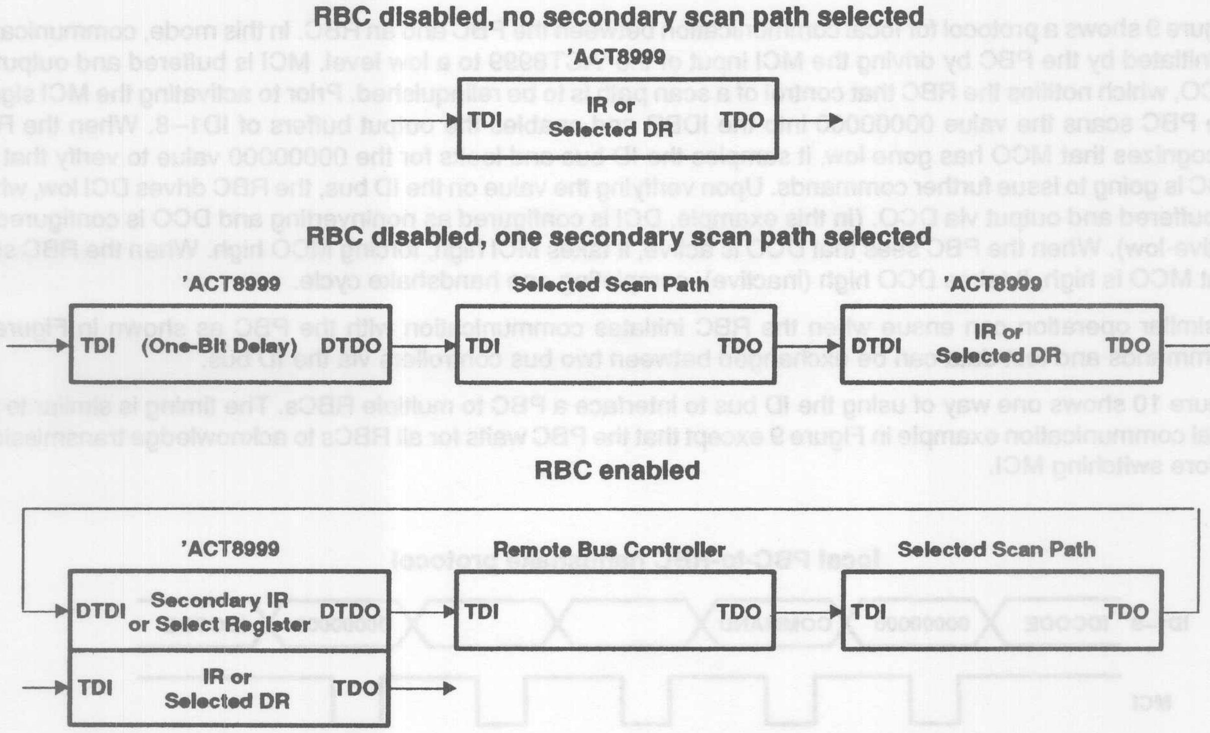


Figure 8. Data Flow in the 'ACT8999

bus communication protocol

The 8-bit identification bus (ID1–8) allows data transfer between a PBC and an RBC. Control register bit 2 configures the 'ACT8999 to transmit or receive command and test data via the ID bus register. The DCI, DCO, MCI, and MCO pins are used to signal the PBC and RBC(s) that a data transfer is required. The 'ACT8999 can accommodate either local or global handshake protocol depending on the number of DCO inputs that the PBC can accommodate.

Figure 9 shows a protocol for local communication between the PBC and an RBC. In this mode, communication is initiated by the PBC by driving the MCI input of the 'ACT8999 to a low level. MCI is buffered and output on MCO, which notifies the RBC that control of a scan path is to be relinquished. Prior to activating the MCI signal, the PBC scans the value 00000000 into the IDBR and enables the output buffers of ID1–8. When the RBC recognizes that MCO has gone low, it samples the ID bus and looks for the 00000000 value to verify that the PBC is going to issue further commands. Upon verifying the value on the ID bus, the RBC drives DCI low, which is buffered and output via DCO. (In this example, DCI is configured as noninverting and DCO is configured as active-low). When the PBC sees that DCO is active, it takes MCI high, forcing MCO high. When the RBC sees that MCO is high, it takes DCO high (inactive), completing one handshake cycle.

A similar operation can ensue when the RBC initiates communication with the PBC as shown in Figure 9. Commands and test data can be exchanged between two bus controllers via the ID bus.

Figure 10 shows one way of using the ID bus to interface a PBC to multiple RBCs. The timing is similar to the local communication example in Figure 9 except that the PBC waits for all RBCs to acknowledge transmissions before switching MCI.

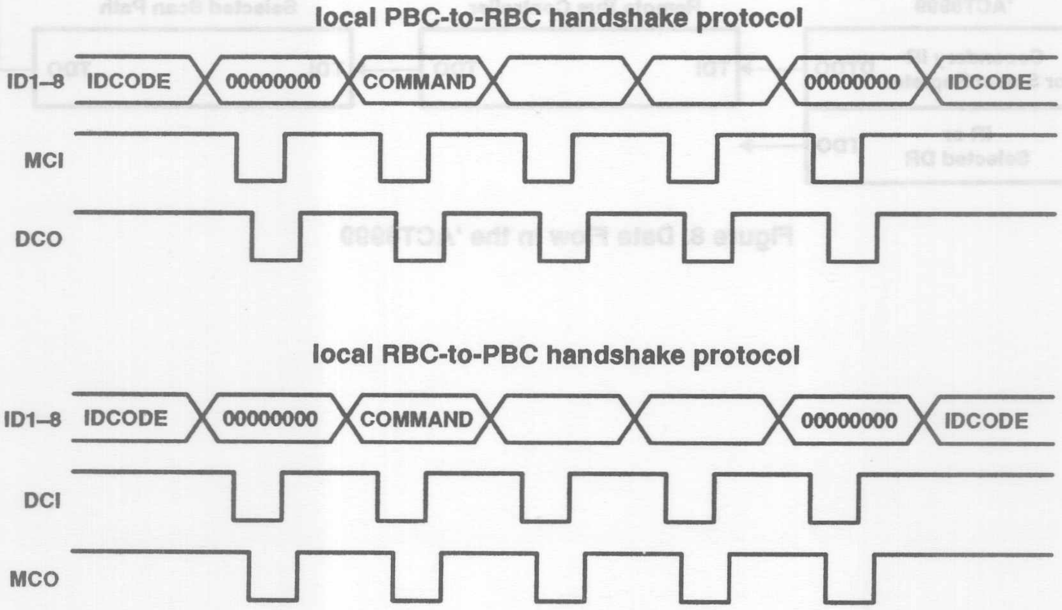


Figure 9. Local Bus Communication Protocol

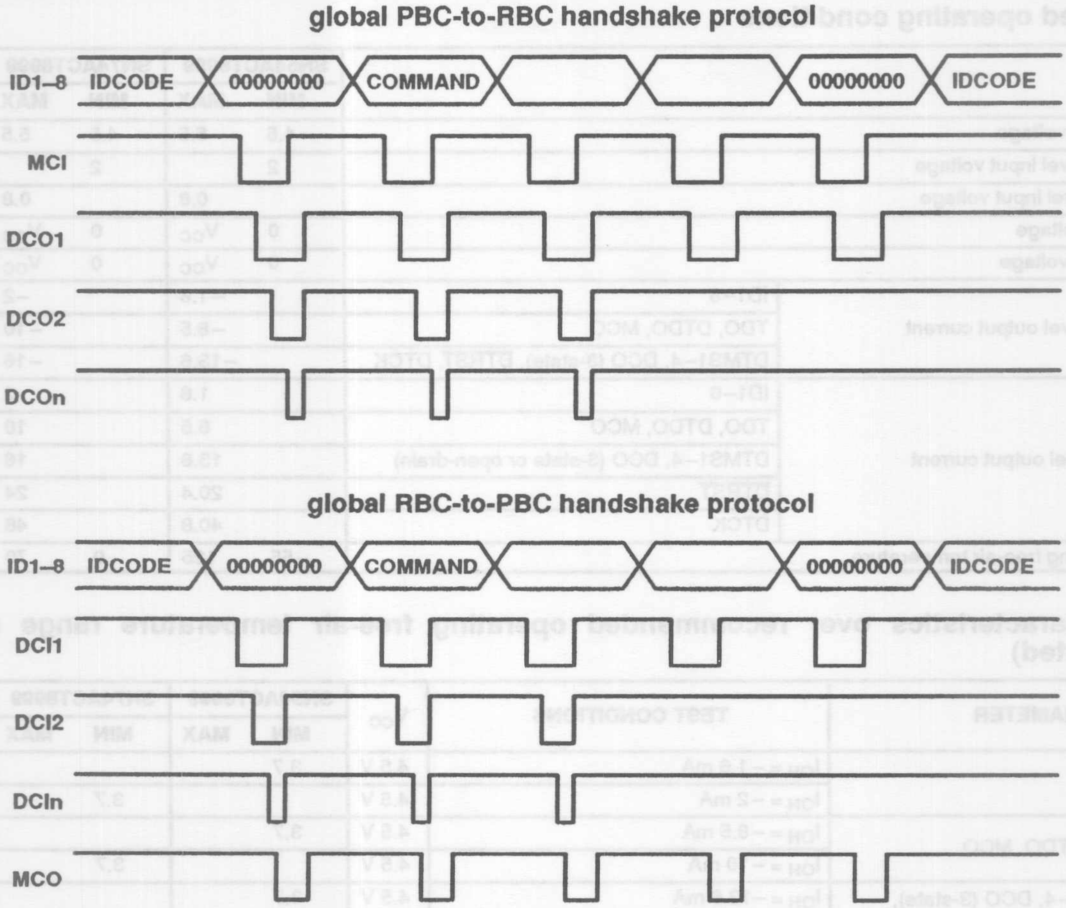


Figure 10. Global Bus Communication Protocol

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.

recommended operating conditions

			SN54ACT8999		SN74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	ID1–8		–1.6		–2	mA
		TDO, DTDO, MCO		–8.5		–10	
		DTMS1–4, DCO (3-state), $\overline{\text{DTRST}}$, DTCK		–13.6		–16	
I_{OL}	Low-level output current	ID1–8		1.6		2	mA
		TDO, DTDO, MCO		8.5		10	
		DTMS1–4, DCO (3-state or open-drain)		13.6		16	
		$\overline{\text{DTRST}}$		20.4		24	
		DTCK		40.8		48	
T_A	Operating free-air temperature		–55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54ACT8999		SN74ACT8999		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	ID1–8	I_{OH} = –1.6 mA	4.5 V	3.7				V
		I_{OH} = –2 mA	4.5 V			3.7		
	TDO, DTDO, MCO	I_{OH} = –8.5 mA	4.5 V	3.7				
		I_{OH} = –10 mA	4.5 V			3.7		
	DTMS1–4, DCO (3-state), $\overline{\text{DTRST}}$, DTCK	I_{OH} = –13.6 mA	4.5 V	3.7				
		I_{OH} = –16 mA	4.5 V			3.7		
V_{OL}	ID1–8	I_{OL} = 1.6 mA	4.5 V		0.5			V
		I_{OL} = 2 mA	4.5 V				0.5	
	TDO, DTDO, MCO	I_{OL} = 8.5 mA	4.5 V		0.5			
		I_{OL} = 10 mA	4.5 V				0.5	
	DTMS1–4, DCO (3-state or open-drain)	I_{OL} = 13.6 mA	4.5 V		0.5			
		I_{OL} = 16 mA	4.5 V				0.5	
	$\overline{\text{DTRST}}$	I_{OL} = 20.4 mA	4.5 V		0.5			
		I_{OL} = 24 mA	4.5 V				0.5	
	DTCK	I_{OL} = 40.8 mA	4.5 V		0.5			
		I_{OL} = 48 mA	4.5 V				0.5	
I_{OZ}†	ID1–8, DTDO, DTMS1–4, DCO, DTCK	$V_O = V_{CC}$ or GND	5.5 V		±10		±5	µA
I_{OH}	DCO (open-drain)	$V_O = V_{CC}$	5.5 V		20		10	µA
I_I	MCI, DCI, TCK	$V_I = V_{CC}$ or GND	5.5 V		±1		±1	µA
	TDI, DTDI, TMS, OTMS, $\overline{\text{TRST}}$	$V_I = V_{CC}$	5.5 V		±1		±1	
		V_I = GND	5.5 V	–0.1	–20	–0.1	–20	
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		100		100	µA
ΔI_{CC}‡		One input at V_I = 3.4 V, Other inputs at V_{CC} or GND	5.5 V		1		1	mA

† For I/O pins, the parameter I_{OZ} includes the input leakage current. For the DCO pin, the parameter I_{OZ} includes the open-drain output leakage current.

‡ This is the increase in supply current for each input being driven at TTL levels rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			SN54ACT8999		SN74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	20	0	20	MHz
		DCI (count mode)	0	20	0	20	
t_w	Pulse duration	TCK high or low	16		16		ns
		DCI high or low (count mode)	9		9		
		TRST low	10		10		
t_{su}	Setup time	TMS before TCK↑	9		9		ns
		OTMS before TCK↑	12		12		
		TDI before TCK↑	11		11		
		DTDI before TCK↑	5		5		
		MCI before TCK↑	5		5		
		DCI before TCK↑	9		9		
		Any ID before TCK↑	3		3		
t_h	Hold time	TMS after TCK↑	2		2		ns
		OTMS after TCK↑	2		2		
		TDI after TCK↑	4		4		
		DTDI after TCK↑	4		4		
		MCI after TCK↑	5		5		
		DCI after TCK↑	5		5		
		Any ID after TCK↑	5		5		
t_d	Delay time	Power up to TCK↑	100*		100		ns

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

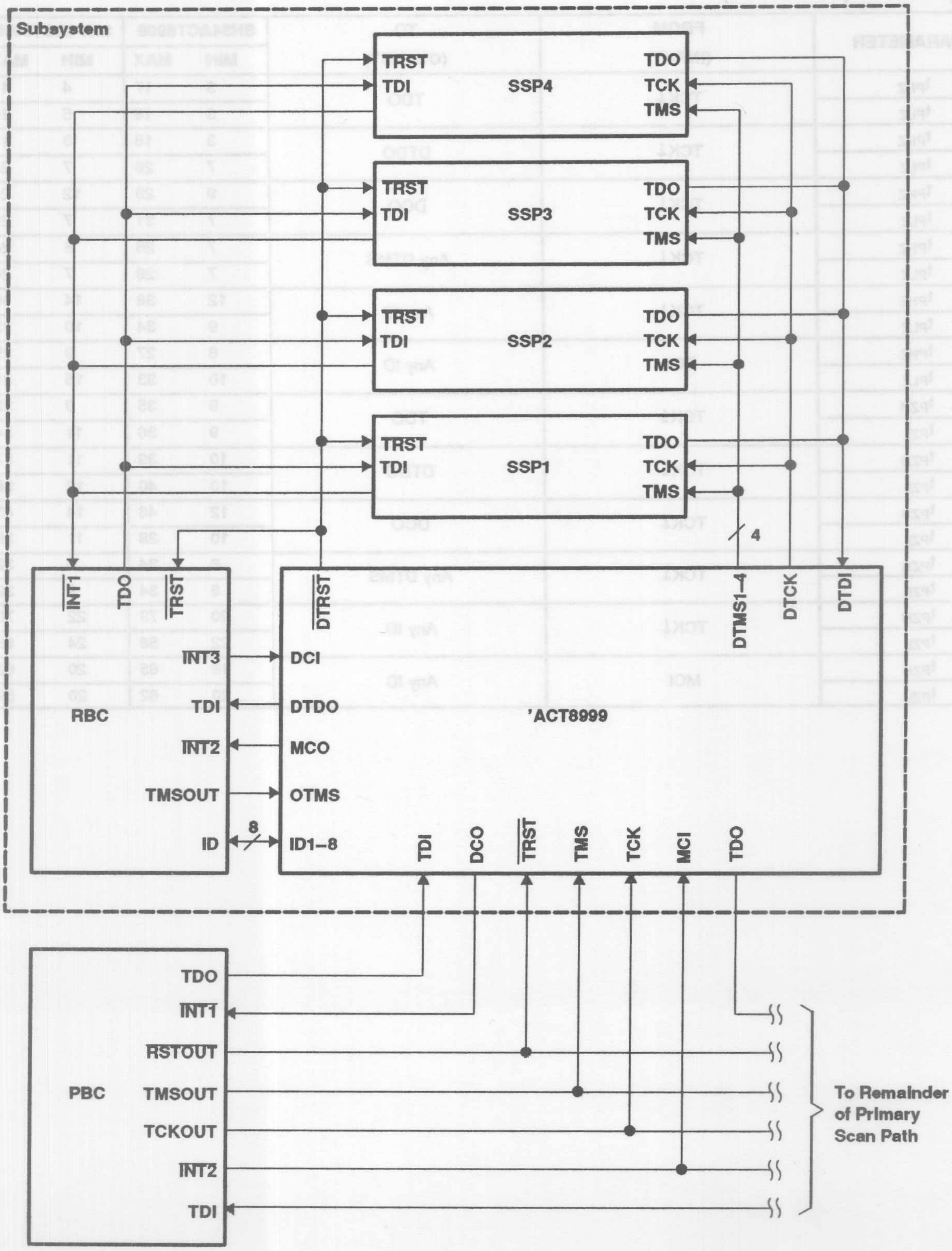
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 11 and 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8999 MIN	SN54ACT8999 MAX	SN74ACT8999 MIN	SN74ACT8999 MAX	UNIT
f_{max}	TCK		20		20		MHz
	DCI (count mode)		20		20		
t_{PLH}	TCK	TDO	7	30	7	28	ns
t_{PHL}			7	29	8	27	
t_{PLH}	TCK↓	$\overline{\text{DTRST}}$	9	35	10	33	ns
t_{PHL}			9	35	10	33	
t_{PLH}	TCK↓	Any DTMS	11	40	11	38	ns
t_{PHL}			11	37	11	35	
t_{PLH}	TCK↓	DTDO	7	31	7	29	ns
t_{PHL}			7	29	8	27	
t_{PLH}	TCK↓	Any ID	20	64	22	61	ns
t_{PHL}			22	65	24	62	
t_{PLH}	TCK↓	MCO	9	34	9	32	ns
t_{PHL}			9	31	9	29	
t_{PLH}	TCK↓	DCO (open-drain)	14	45	18	42	ns
		DCO (3-state)	10	40	11	38	
t_{PHL}	TCK↓	DCO (open-drain)	10	39	11	37	ns
		DCO (3-state)	10	37	11	35	
t_{PLH}	TMS	Any DTMS	5	22	6	20	ns
t_{PHL}			4	23	5	21	
t_{PLH}	OTMS	Any DTMS	5	22	6	20	ns
t_{PHL}			4	23	5	21	
t_{PLH}	MCI	MCO	7	26	8	24	ns
t_{PHL}			6	25	7	23	
t_{PLH}	DCI	DCO (open-drain)	8	32	9	30	ns
		DCO (3-state)	8	30	10	28	
t_{PHL}	DCI	DCO (open-drain)	8	34	9	32	ns
		DCO (3-state)	8	30	9	28	
t_{PLH}	$\overline{\text{TRST}}$	$\overline{\text{DTRST}}$	4	20	5	18	ns
t_{PHL}			5	25	6	23	
t_{PLH}	TCK	DTCK	3	16	3	14	ns
t_{PHL}			3	19	3	17	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8999 MIN	SN54ACT8999 MAX	SN74ACT8999 MIN	SN74ACT8999 MAX	UNIT
t_{PHZ}	TCK↓	TDO	3	17	4	15	ns
t_{PLZ}			3	18	5	16	
t_{PHZ}	TCK↓	DTDO	3	18	3	16	ns
t_{PLZ}			7	26	7	24	
t_{PHZ}	TCK↓	DCO	9	28	12	26	ns
t_{PLZ}			7	31	7	29	
t_{PHZ}	TCK↓	Any DTMS	7	26	8	24	ns
t_{PLZ}			7	28	7	26	
t_{PHZ}	TCK↓	Any ID	12	38	14	36	ns
t_{PLZ}			9	34	10	32	
t_{PHZ}	DCI	Any ID	8	27	9	25	ns
t_{PLZ}			10	33	15	31	
t_{PZH}	TCK↓	TDO	9	35	9	33	ns
t_{PZL}			9	36	11	34	
t_{PZH}	TCK↓	DTDO	10	39	11	37	ns
t_{PZL}			10	40	12	38	
t_{PZH}	TCK↓	DCO	12	46	14	43	ns
t_{PZL}			10	38	11	36	
t_{PZH}	TCK↓	Any DTMS	8	34	9	32	ns
t_{PZL}			8	34	9	32	
t_{PZH}	TCK↓	Any ID	20	73	22	70	ns
t_{PZL}			22	58	24	65	
t_{PZH}	MCI	Any ID	18	65	20	62	ns
t_{PZL}			20	62	20	59	

APPLICATION INFORMATION



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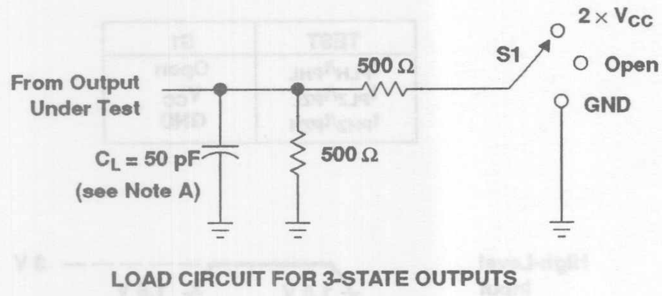
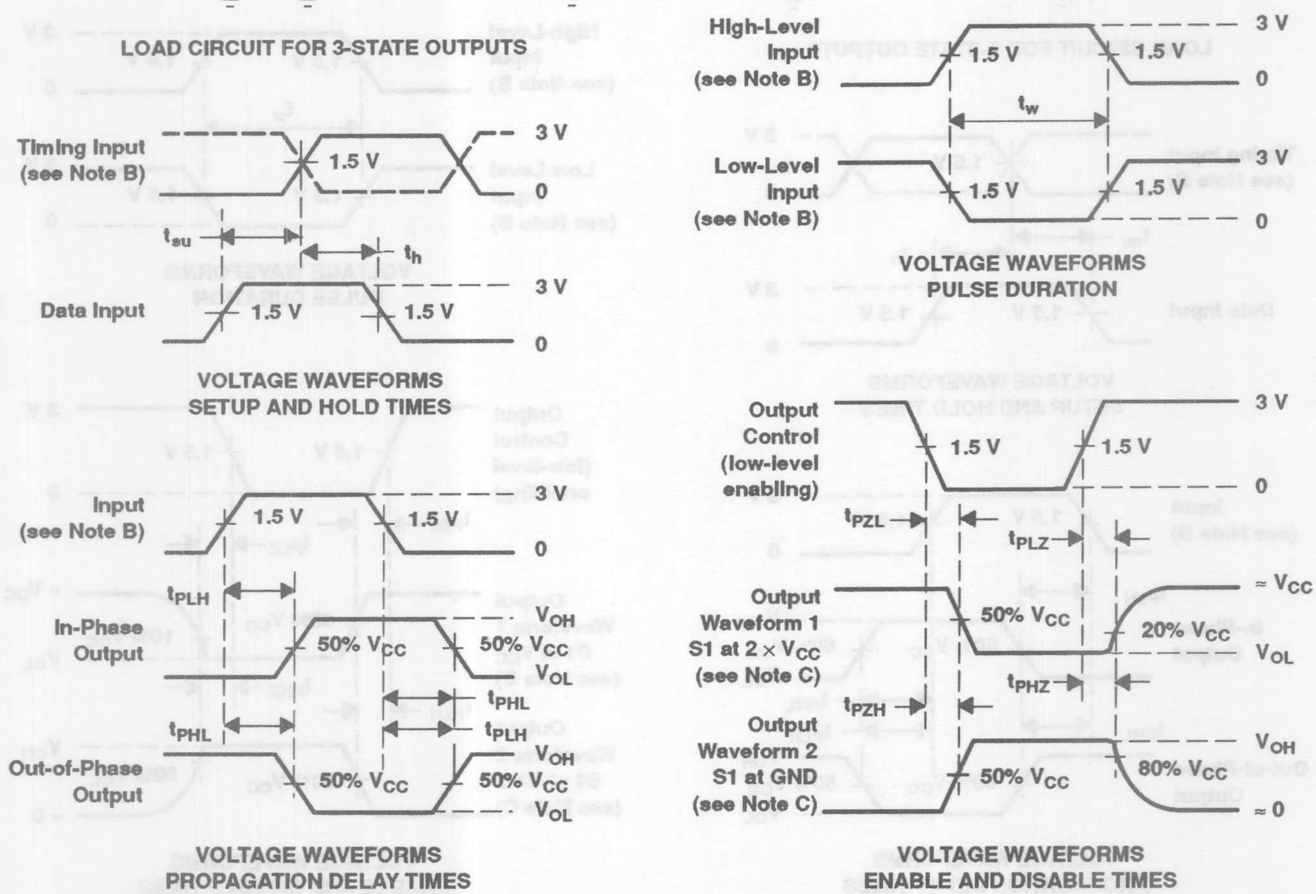
PARAMETER MEASUREMENT INFORMATION



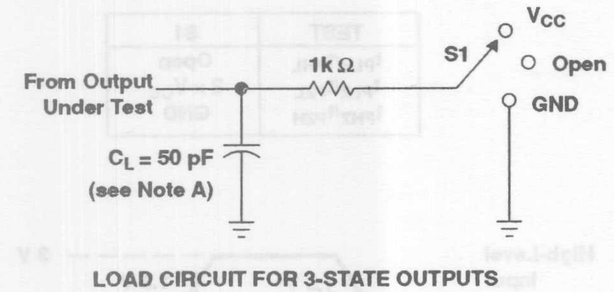
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



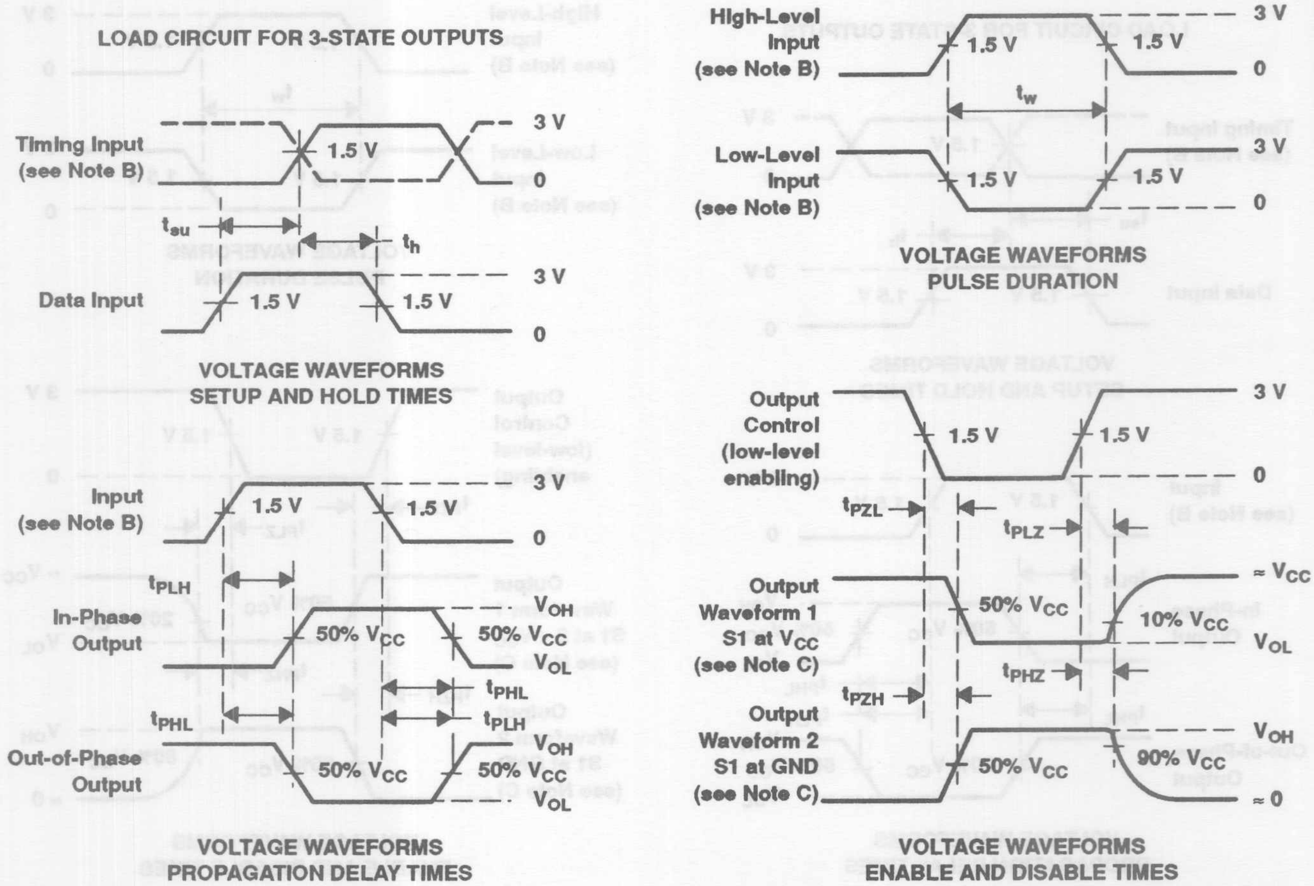
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 11. Load Circuit and Voltage Waveforms (For All Pins Except ID Bus Pins)

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

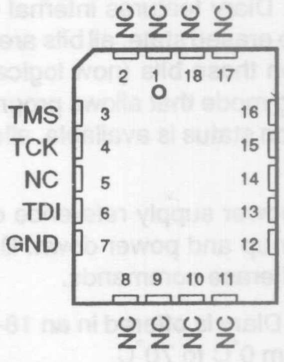


NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 12. Load Circuit and Voltage Waveforms (ID Bus Pins Only)

- **Member of Texas Instruments *SCOPE*™ Family of Testability Products**
- **IEEE 1149.1 Serial Test Bus Compatible**
- **Organization . . . 2048 × 8-Bit Flash Memory**
- **TCK Frequency (V_{CC} ± 10%)**
  '29F816-06 6.25 MHz
- **5-V Program/Erase/Read Operation**
- **4 Flash-Erasable Blocks (128-, 384-, 512-, and 1024-Byte Size)**
- **Software Sequence Write/Erase Protection**
- **Lockbits**
- **Self-Timed Write/Erase Cycles**
- **Streaming Read/Write Modes**
- **32-Byte Page Programming Mode**
- **CMOS Technology**
- **Single 5-V Power Supply (± 10% Tolerance)**
- **18-Pin Plastic Leaded-Chip Carrier (FM) Package**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
TMS	Test Mode Select
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
DLA	Disable Lock A
DLB	Disable Lock B
V_{CC}	5-V Power Supply
GND	Ground
NC	No internal connection

description

The SCOPE Diary is a 16 384-bit, programmable storage device that can be electrically block-erased and reprogrammed. The SCOPE Diary is fabricated using HVCMOS FLOTOX technology for high reliability and very low power dissipation. It performs the erase/program operations automatically with a single 5-V supply voltage, and it can program a single byte or up to 32 bytes in one cycle.

All SCOPE Diary operations are accomplished via a 4-wire Test Access Port (TAP) interface. This interface complies with the IEEE 1149.1 Serial Test Bus standard (JTAG). The interface consists of two control signals: Test Mode Select (TMS) and Test Clock (TCK); and two test data pins: Test Data In (TDI) and Test Data Out (TDO). The JTAG Test Access Protocol defines how this 4-wire test bus is used to scan in instructions and data, execute instructions, and scan out the resulting data.

All test information is serially loaded into the chip via TDI and out of the chip via TDO. Three mandatory JTAG components are added to the Flash EEPROM array: a TAP controller, a set of test data registers, and an instruction register.

The TAP controller interfaces both the test data registers and the instruction register to the 4-wire test bus. The test data registers load and/or capture test data. The instruction register selects the test data register(s) to be accessed and the test to be performed. There are three types of test data registers: the Data Scan Registers (DSR), the Bypass Register (BR), and the Device Identification Register (IDR).

The SCOPE Diary is divided into four independently flash-erasable blocks. These blocks are configured as 128, 384, 512, and 1024 bytes in size. These blocks can be prevented from being programmed or erased by programming any or all of the four write-once lockbits.

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description (continued)

The SCOPE Diary features internal circuitry for self-timed programming, self-timed erasing, and completion polling. In the erased state, all bits are at a logical 1. To reprogram, all memory bits in a selected block are erased first, and then those bits (now logical 1s) are programmed accordingly. The SCOPE Diary supports a page programming mode that allows programming of up to 32 bytes in one cycle. During programming and erasing, the completion status is available, allowing the system to begin a new operation before the maximum specified timeout.

An on-chip power supply reference comparator protects the SCOPE Diary from write and erase commands during power up and power down. During normal operation, software sequences protect against inadvertent program and erase commands.

The SCOPE Diary is offered in an 18-pin plastic leaded-chip carrier package (FM suffix). It is characterized for operation from 0°C to 70°C.

The SCOPE Diary is available in a 1000-cycle endurance version.

terms

clock

The term *clock* refers to the system test clock used by the controller and its target(s). The clock is input on TCK.

DMA

The SCOPE Diary supports the Direct Memory Access (DMA) extension to the 1149.1 standard. The DMA mode enables a continuous stream of bits to be scanned in or out of the SCOPE Diary.

host

The term *host* refers to the device directing the activity of the SCOPE Diary.

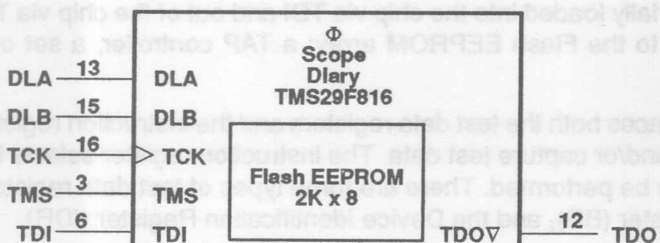
JTAG

The Joint Test Action Group (JTAG) is the originator of IEEE Standard 1149.1.

SCOPE

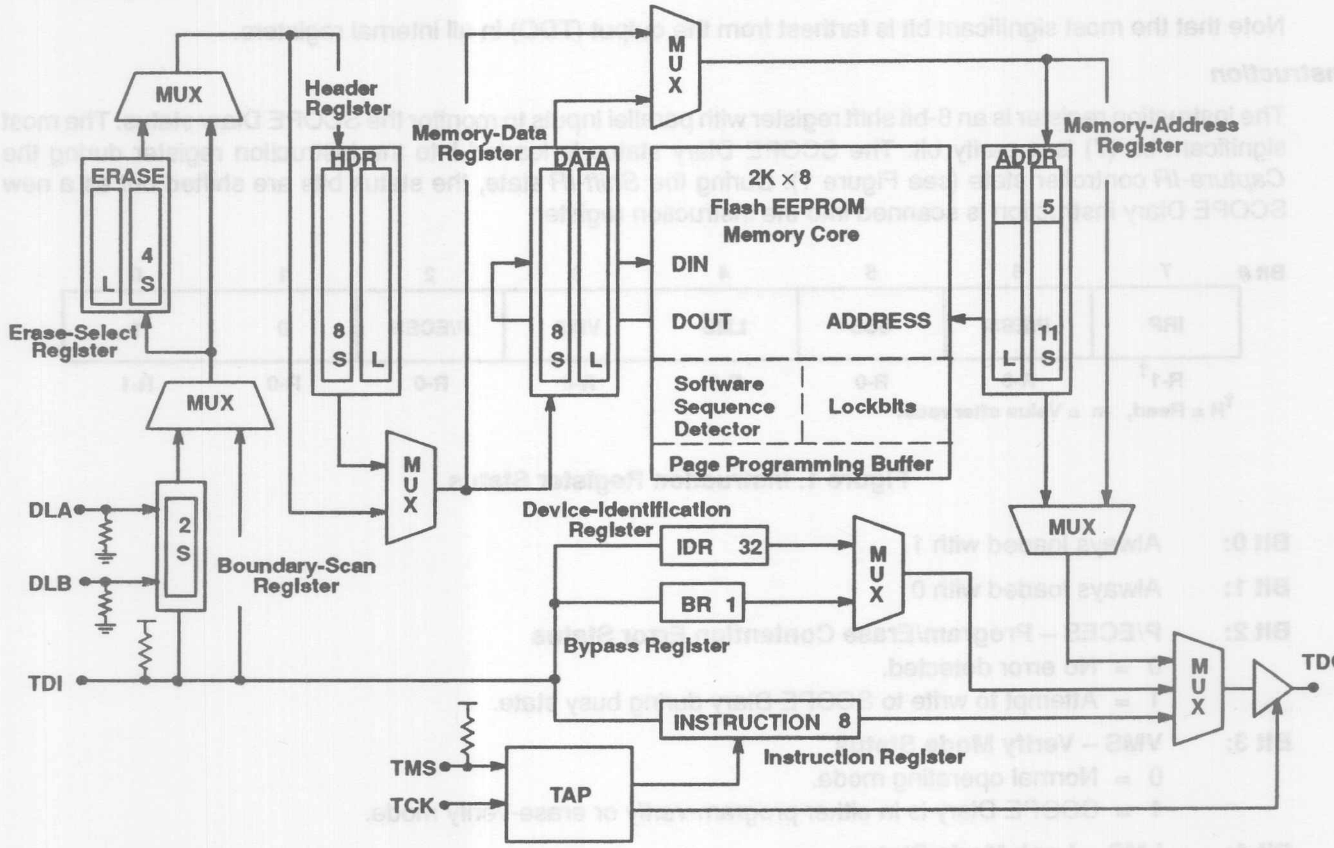
System Controllability and Observability Partitioning Environment (SCOPE) is the family name for Texas Instruments testability products.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



pin names and functions

Pin Name	Pin #	I/O	Description
TMS	3	I	Test Mode Select. Controls transition of TAP finite state machine. This input is sampled on the rising edge of TCK.
TCK	4	I	Test Clock. Input clock to TAP finite state machine. All changes in state are synchronous to the test clock TCK.
TDI	6	I	Test Data In. Data input to the internal register scan path. Data on this pin is sampled on the rising edge of TCK.
TDO	12	O	Test Data Out. Data output from the internal register scan path. Data is updated on this pin on the falling edge of TCK.
DLA	13	I	Disable Lock A. Controls lockbit functionality for memory array block 0. When DLA = V_{IL}, the state of lockbit 0 (LCK0) determines whether block 0 can be erased or programmed. When DLA = V_{IH}, block 0 can be erased or programmed regardless of the state of lockbit 0. When DLA = V_H ($V_H >> V_{CC}$), the SCOPE Diary enters a special manufacturing test mode.
DLB	15	I	Disable Lock B. Controls lockbit functionality for memory blocks 1, 2, and 3. When DLB = V_{IL}, the states of lockbits 1, 2, and 3 (LCK1, LCK2, LCK3) determine whether their respective blocks (1, 2, and 3) can be erased or programmed. When DLB = V_{IH}, blocks 1, 2, and 3 can be erased or programmed, regardless of the state of their associated lockbits.
V_{CC}	16	I	5-V Power Supply. (± 10% operating power supply connection.)
GND	7	I	Ground reference

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internal registers

Note that the most significant bit is farthest from the output (TDO) in all internal registers.

instruction

The instruction register is an 8-bit shift register with parallel inputs to monitor the SCOPE Diary status. The most significant bit (7) is a parity bit. The SCOPE Diary status is loaded into the instruction register during the *Capture-IR* controller state (see Figure 1). During the *Shift-IR* state, the status bits are shifted out as a new SCOPE Diary instruction is scanned into the instruction register.

Bit #	7	6	5	4	3	2	1	0
	IRP	P/EBS	SSS	LMS	VMS	P/ECES	0	1
	R-1†	R-0	R-0	R-0	R-0	R-0	R-0	R-1

†R = Read, -n = Value after reset

Figure 1. Instruction Register Status

Bit 0: Always loaded with 1.

Bit 1: Always loaded with 0

Bit 2: **P/ECES – Program/Erase Contention Error Status**
0 = No error detected.
1 = Attempt to write to SCOPE Diary during busy state.

Bit 3: **VMS – Verify Mode Status**
0 = Normal operating mode.
1 = SCOPE Diary is in either program-verify or erase-verify mode.

Bit 4: **LMS – Lock Mode Status**
0 = Normal operating mode.
1 = SCOPE Diary is in lockbit mode.

Bit 5: **SSS – Software Sequence Status**
0 = Normal operating mode.
1 = Valid software sequence detected. The bit will be set within 2 µs after the SCOPE Diary detects a valid software sequence. The bit will remain set until one of the following occurs:
a) The sequence timer expires.
b) The active program or erase cycle is complete.
c) The CLRSWS command is issued.

Bit 6: **P/EBS – Program/Erase Busy Status**
0 = Normal operating mode.
1 = Busy state. The SCOPE Diary is executing a self-timed program or erase operation. The bit will be set within 2 µs after the BEGOPS instruction is executed. This bit will remain set until the operation is complete.

Bit 7: **IRP – Instruction Register Parity**
All valid commands to the instruction register are even parity.
0 = Parity error detected in previously loaded instruction. The SCOPE Diary will automatically place the BYPASS register into the data register scan path.
1 = No parity error in previously loaded instruction.

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internal registers (continued)

boundary-scan

The boundary-scan register is a 2-bit register. Bit 0 of this register is connected to DLA; bit 1 is connected to DLB. This register can only be used to sample the connected inputs; therefore, values stored in the boundary-scan register during the *Update-DR* controller state will not be applied to the internal core logic.

device-identification

The device identification register returns the following 32-bit code when interrogated with the IDCODE command: *0000102Fh*. The device ID register is selected into the scan path during power-on reset or upon entering the *Test-Logic-Reset* state.

bypass

The bypass register is a 1-bit register. It allows data to transfer from TDI to TDO in one TCK clock cycle. The bypass register is selected into the scan path when a parity error is detected during the *Shift-IR* state.

memory-data

The memory-data register is an 8-bit register used to load data into the memory array during write operations. This register is also used to sample data from the memory array during read operations. The parallel-scan load path is connected to the memory core data outputs. The output of the register latch is connected to the data input of the memory core. The operation of the register is shown in Table 1.

Table 1. Memory-Data Register Operation

Opcode	Capture-DR	Shift-DR	Update-DR
DMARD	Memory Data to Scan	Data Stream from Array	Scan to Register Latch
DMAWR	Memory Data to Scan	Data Stream to Array	Scan to Register Latch
BYTERD	Memory Data to Scan	Normal Shift Operation	Scan to Register Latch
BYTEWR	Memory Data to Scan	Normal Shift Operation	Scan to Register Latch
ISTEST	Register Latch to Scan	Normal Shift Operation	Scan to Register Latch

memory-address

The memory-address register is a 16-bit register used to address the Flash EEPROM array during read and write operations. Bits 10 – 0 are used to address the Flash memory array. Bits 14 – 0 are used to address the software sequence detector. The operation of the register is shown in Table 2.

Table 2. Memory-Address Register Operation

Opcode	Capture-DR	Shift-DR	Update-DR
LDADDR	Register Latch to Scan	Normal Operation	Scan to Register Latch
DMARD	Hold	Auto-Increment	Hold
DMAWR	Hold	Data Stream to Array	Hold
BYTERD	Register Latch to Scan	Normal Operation	Scan to Register Latch
BYTEWR	Register Latch to Scan	Normal Operation	Scan to Register Latch
ISTEST	Register Latch to Scan	Normal Operation	Scan to Register Latch

ADVANCE INFORMATION

internal registers (continued)

page programming buffer

The programming pages begin on 32-byte boundaries. Data being written to the SCOPE Diary is stored in the 32-byte page programming buffer until the memory-array programming cycle begins. The page buffer address mechanism does not automatically recognize page programming buffer loads that cross a page boundary. Bits 10 – 5 of the last address presented to the page programming buffer will be used as the page pointer when the memory array programming cycle begins. After an initial data value is loaded into the page programming buffer, all remaining bytes within the page programming buffer are initialized to FFh.

erase-select

The erase-select register is a 4-bit register used to select the Flash memory block(s) that will be erased during an erase cycle. Each bit in the register maps to one of the memory blocks (see Figure 2). To select a block for erasure, set the block's corresponding memory-control bit to logic 1. The operation of the register is shown in Table 3.

Bit #	3	2	1	0
	Block 3	Block 2	Block 1	Block 0
	RW-0†	RW-0	RW-0	RW-0

†R = Read, W = Write, -n = Value after reset

Figure 2. Erase-Select Register

Bit 0: **Block 0 Erase Enable (address 0000 – 007F)**
0 = Erase disable
1 = Erase enable

Bit 1: **Block 1 Erase Enable (address 0080 – 01FF)**
0 = Erase disable
1 = Erase enable

Bit 2: **Block 2 Erase Enable (address 0200 – 03FF)**
0 = Erase disable
1 = Erase enable

Bit 3: **Block 3 Erase Enable (address 0400 – 07FF)**
0 = Erase disable
1 = Erase enable

Table 3. Erase-Select Register Operation

Opcode	Capture-DR	Update-DR
ERABLK	Register Latch to Scan	Scan to Register Latch
ISTEST	Register Latch to Scan	Scan to Register Latch

ADVANCE INFORMATION

internal registers (continued)

lockbits

The lockbit register contains *four one-time-programmable, non-erasable bits.* The lockbits map one-to-one to the blocks in the array (bit 0 maps to block 0). The lockbit register is not located on the scan path; it is internal to the memory core. It can be accessed using the memory-address and memory-data registers.

To prevent a block from being programmed or erased, program a logic 0 in the block's corresponding bit position. Read and write operations to the lockbits are selected by the SETLOCK instruction. To program the lockbits, execute the DMAWR or BYTEWR instruction sequences while in the lock mode. The lockbit register is shown in Figure 3.

Bit #	3	2	1	0
	Block 3	Block 2	Block 1	Block 0
	RW-1†	RW-1	RW-1	RW-1

† R = Read, W = Write, -n = Initial value

Figure 3. Lockbit Register

Bit 0: **Block 0 Lock Enable (address 0000 – 007F)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 1: **Block 1 Lock Enable (address 0080 – 01FF)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 2: **Block 2 Lock Enable (address 0200 – 03FF)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 3: **Block 3 Lock Enable (address 0400 – 07FF)**
0 = Block program and erase disable
1 = Block program and erase enable

header

The header register is an 8-bit register used to control the mode of operation during a DMAWR instruction. The register is cleared to zero on power up and upon entering the *Test-Logic-Reset* state. When the register is cleared (all bits to logic 0), the SCOPE Diary uses a state-transition mode to synchronize the DMA write operation. If the register is not cleared, the contents will be used as a shift data input pattern match to synchronize the start of the DMA write operation.

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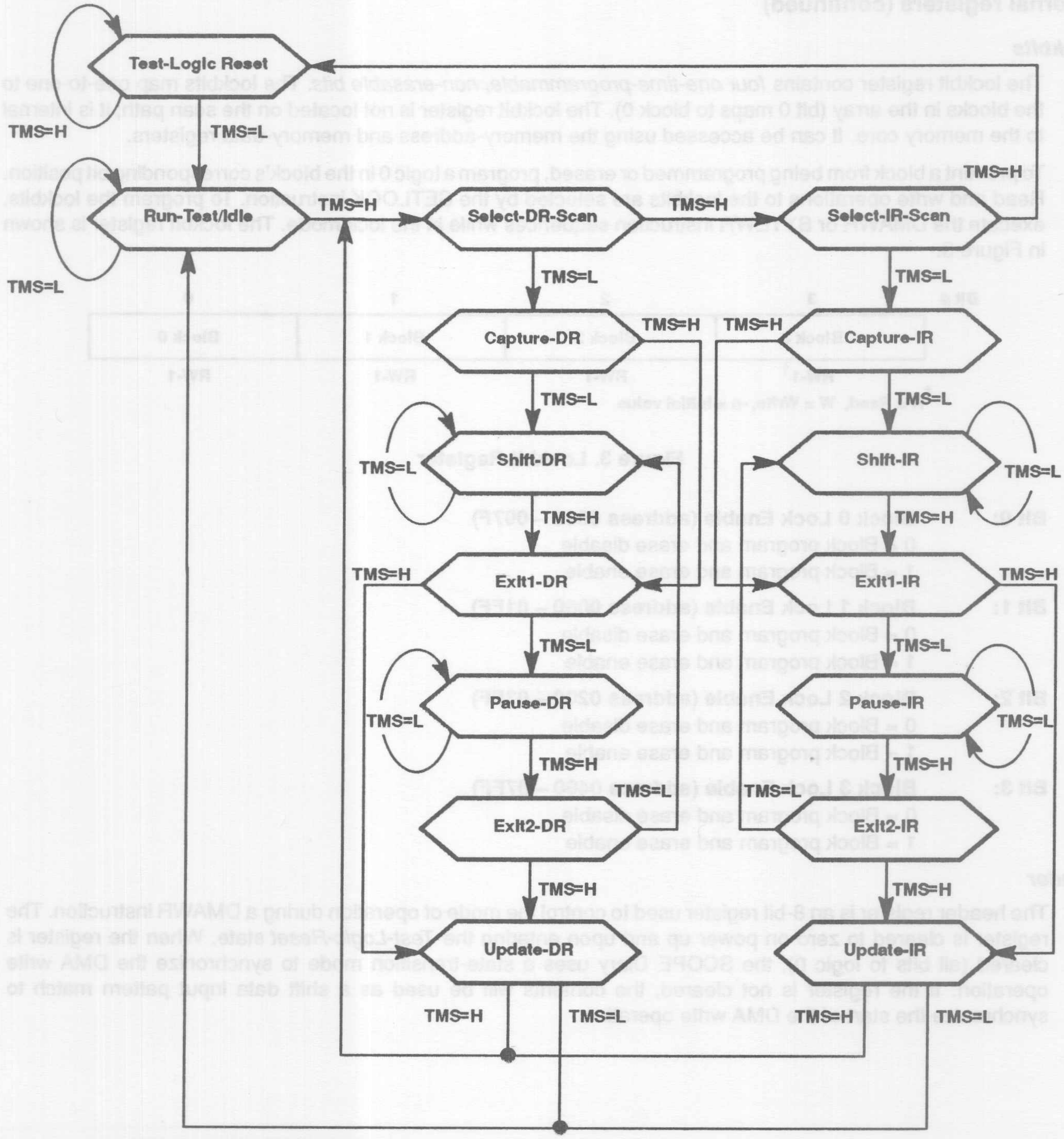

Figure 4. TAP State Diagram

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TAP state diagram description (see Figure 4)

The SCOPE Diary TAP controller accepts TCK and TMS signals compatible with IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten transient states (indicated by two exiting arrows) in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any other state is a transient state.

There are two main paths through the state diagram; one accesses selected data registers, and one accesses the instruction register.

Test-Logic-Reset

In this state, the test logic is inactive, and an internal reset signal is applied to all registers in the SCOPE Diary. During SCOPE Diary operation, the TAP returns to the *Test-Logic-Reset* state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level when it is left unconnected or when a board defect causes it to be open-circuited.

Run-Test/Idle

The TAP *must* pass through this state before executing any test operations. The TAP may retain this state indefinitely. No registers are modified while the SCOPE Diary is in the *Run-Test/Idle* state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states. TAP exits them on the next TCK cycle.

Capture-DR

Selected data registers are placed in the scan path (between TDI and TDO). The current instruction determines whether or not the data is loaded or captured into the scan path. The TAP exits the state on the rising edge of TCK.

Shift-DR

In this state, data is shifted serially through the selected data registers, from TDI to TDO, on each TCK cycle. The first shift occurs after the first TCK cycle after entering this state. (No shifting occurs during the TCK cycle in which the TAP changes from *Capture-DR* to *Shift-DR* or from *Exit2-DR* to *Shift-DR*.)

In *Shift-DR*, on the falling edge of TCK, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the *Test-Logic-Reset* state since the last scan operation, TDO enables to the level present before it was last disabled. If the TAP has passed through the *Test-Logic-Reset* state since the last operation, TDO enables to a high level.

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the *Shift-DR* state from either *Exit1-DR* or *Exit2-DR* without recapturing the data registers. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from *Shift-DR* to *Exit1-DR*.

Pause-DR

The TAP can remain in this state indefinitely. The *Pause-DR* state allows you to suspend and resume shift operations without losing data.

Update-DR

In the *Update-DR* state, the current instruction determines whether or not the latches in the selected data registers are updated with data from the scan path.

Capture-IR

In the *Capture-IR* state, the instruction register is preloaded with the IR status word, and then it is placed in the scan path. The TAP exits the state on the rising edge of TCK.

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TAP state diagram description (continued)

Shift-IR

In this state, data is shifted serially through the instruction register, from TDI to TDO, on each TCK cycle. The first shift occurs after the first TCK cycle after entering this state. (No shifting occurs during the TCK cycle in which the TAP changes from *Capture-IR* to *Shift-IR* or from *Exit2-IR* to *Shift-IR*.) In *Shift-IR*, on the falling edge of TCK, TDO goes from the high-impedance state to the active state.

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the *Shift-IR* state from either *Exit1-IR* or *Exit2-IR* without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from *Shift-IR* to *Exit1-IR*.

Pause-IR

The TAP can remain in this state indefinitely. The *Pause-IR* state allows you to suspend and resume shift operations without losing data.

Update-IR

In the *Update-IR* state, the instruction register latches are updated with the new instruction from the scan path.

Instructions

standard SCOPE instructions

The SCOPE Diary supports a subset of the standard SCOPE instruction set. The defined instructions are shown in Table 4. All other SCOPE instructions select the default BYPASS instruction.

Table 4. Standard SCOPE Instructions

Opcode	Code	Description
BYPASS	FFh	Select Bypass Register
EXTEST	00h	External Boundary Test (see Note 1)
IDCODE	81h	ID Register Scan
SAMPLE	82h	Boundary Sample

NOTE 1: During operation, the EXTEST instruction behaves identically to the SAMPLE instruction.

SCOPE Diary-specific instructions

The SCOPE Diary supports specific instructions to control the operation of the Flash EEPROM array. The defined instructions are shown in Table 5. All undefined opcodes select the BYPASS instruction.

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Instructions (continued)

Table 5. SCOPE Diary-Specific Instructions

Opcode	Code	Description
BEGOPS	69h	Begin Operation in Progress
BYTERD	63h	Byte Read
BYTEWR	E4h	Byte Write
CLRERR	6Ah	Clear Conflict Error Flag
CLRLOCK	66h	Exit Lock Mode
CLRSWS	EBh	Clear Software Sequence
DMARD	E1h	DMA Read
DMAWR	E2h	DMA Write
ERABLK	E7h	Erase Block Register Select
ISTEST	6Ch	Internal Self Test
LDADDR	60h	Load Address Register
LOADHDR	E8h	Header Register Select
SETLOCK	65h	Enter Lock Mode

BEGOPS Begin Operation in Progress

Scan Path TDI → bypass → TDO

Description The BEGOPS instruction is used to initiate a program, erase, or verify mode operation after the appropriate software sequence has been issued. This instruction must be executed within 9 ms of the last write operation, and the software sequence status bit in the instruction register must be set, or the selected operation will not begin. If the time-out condition is not met, the software sequence commands must be re-issued. Once the BEGOPS instruction is loaded, it is not executed until the diary is placed in the *Run-Test/Idle* state.

BYPASS Select Bypass Register

Scan Path TDI → bypass → TDO

Description The BYPASS instruction conforms to the 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register during the *Update-DR* state.

BYTERD Byte Read

Scan Path TDI → memory-data → memory-address → TDO

Description The BYTERD instruction is used to read the value stored in a memory array location. During the read operation, the contents of the memory-address register point to the value. This value is captured in the memory-data register during the *Update-DR* state.

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Instructions (continued)

BYTEWR Byte Write

Scan Path TDI → memory-data → memory-address → TDO

Description The BYTEWR instruction performs two operations. It can write 8-bit values into both the software sequence detector and the page programming buffer. The contents of the memory-address register and the contents of the memory-data register are presented to the memory core during the *Update-DR* state. On the rising edge of TCK, upon leaving the *Update-DR* state, an internal write signal is applied to either the software sequence detector or the page programming buffer.

CLRERR Clear Conflict Error Flag

Scan Path TDI → bypass → TDO

Description The CLRERR instruction is used to reset the program/erase conflict flag. The conflict flag (status bit 2 in the instruction register) will be set if any write operations are issued while the SCOPE Diary is programming or erasing. After the conflict flag is set, the SCOPE Diary won't recognize any sequence commands. The conflict flag will remain set until the CLRERR instruction is executed.

CLRLOCK Exit Lock Mode

Scan Path TDI → bypass → TDO

Description The CLRLOCK instruction is used to exit the lock mode. When the lock mode is disabled, all read and programming operations are directed to the memory array. The normal mode is indicated when status bit 4 is cleared in the instruction register.

CLRSWS Clear Software Sequence

Scan Path TDI → bypass → TDO

Description The CLRSWS instruction is used to clear software sequence operations. The instruction will reset or cancel any software sequence up until the BEGOPS instruction is executed. The CLRSWS instruction will also clear status bit 5 (valid software sequence detected) in the instruction register. The CLRSWS instruction will not interrupt an erase or program operation once the operation has started.

DMARD DMA Read

Scan Path TDI → (ignored) / memory-data → TDO

Description The DMARD instruction is used to perform streaming data reads from the Flash EEPROM memory array. During the read operation, upon entering the *Shift-DR* state, the contents of the memory array will be shifted out beginning with the currently addressed location. The memory-address register is automatically incremented on each byte boundary while performing the DMARD operation. Input data on the TDI pin is discarded and does not pass through to the TDO output pin.

ADVANCE INFORMATION

Instructions (continued)

DMAWR DMA Write

Scan Path TDI → memory-data → memory-address → TDO

Description The DMAWR instruction allows a streaming method of writing address/data pairs to the SCOPE Diary. During the *Shift-DR* state, the SCOPE Diary will automatically generate write strobes to the memory core on each 24-bit address/data pair boundary. The SCOPE Diary supports two modes of synchronizing the write operation with the incoming address/data pairs; state-transition mode and stream-header mode. The contents of the header register determine the selected mode.

ERABLK Erase Block Register Select

Scan Path TDI → erase-block → TDO

Description The ERABLK instruction is used to access the erase-block select register. Data loaded into the ERABLK register is presented to the memory core during the *Update-DR* state.

EXTEST External Boundary Test

Scan Test TDI → boundary-scan → TDO

Description The EXTEST instruction is used to check the board connectivity of the DLA and DLB input pins. During an EXTEST operation, DLA and DLB inputs to the internal control logic can be sampled by the scan path, but not driven.

IDCODE ID Register Scan

Scan Path TDI → id → TDO

Description The IDCODE instruction is used to read the device identification data. During the *Capture-DR* state, the 32-bit device identification code (0000102Fh) is loaded into the ID register. The IDCODE instruction is automatically loaded during SCOPE Diary power-on reset or upon entry to the *Test-Logic-Reset* state.

ISTEST Internal Self Test

Scan Path TDI → boundary-scan → erase-block → header → memory-data → memory-address → TDO

Description The ISTEST instruction is used to test scan path data registers. During the *Capture-DR* state, all of the register latched values are transferred to the scan path (except the boundary scan register which transfers the values of DLA and DLB to the scan path).

LDADDR Load Address Register

Scan Path TDI → memory-address → TDO

Description The LDADDR instruction is used to load the memory-address register. The 16-bit value loaded from the scan path points to an address and is presented to the memory array during the *Update-DR* state.

LOADHDR Header Register Select

Scan Path TDI → header → TDO

Description The LOADHDR instruction is used to access the header register. Loading any value from 01h to FFh selects header mode synchronization during DMA write operations. Loading the header register with 00h selects state-transition mode synchronization for DMA write operations. During the LOADHDR operation, the header register is selected into the DR scan path.

ADVANCE INFORMATION

Instructions (continued)

SAMPLE Boundary Sample

Scan Path TDI → boundary-scan → TDO

Description The SAMPLE instruction is used to check the board connectivity of the DLA and DLB input pins. During a SAMPLE operation, DLA and DLB inputs to the internal control logic can be sampled by the scan path, but not driven.

SETLOCK Enter Lock Mode

Scan Path TDI → bypass → TDO

Description The SETLOCK instruction is used to enable the lock mode. When the lock mode is enabled, read and programming operations are directed to the lockbits. The lock mode operation is indicated when status bit 4 is set in the instruction register. The SCOPE Diary will remain in the lock mode until the CLRLOCK instruction is executed. While in the lock mode, all read operations capture the state of the lockbits in the data-memory register. While reading the lockbits, the four most significant bits are set to logic 1.

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operation

TAP state controller

Operation of the TAP state controller conforms to the IEEE 1149.1 Serial Test Bus standard. The state flow diagram is shown in Figure 4 on page 8.

loading and executing instructions

All bus sequences that load and execute instructions start with the TAP in the *Run-Test/Idle* state. To initialize the TAP to *Run-Test/Idle* from any other state, apply the 6-cycle sequence shown in Table 6.

Table 6. TAP Reset Sequence

Cycle	1	2	3	4	5	6
TMS	1	1	1	1	1	0
TCK						
TDI†	X	X	X	X	X	X
TDO	(See Note 2)	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
TAP State	Undefined	Undefined	Undefined	Undefined	Test-Logic-Reset	Run-Test/ Idle

† X denotes a don't care.

NOTE 2: TDO will become high-impedance on falling edge of TCK.

sequence timing

The SCOPE Diary contains internal timing logic to simplify programming and erase operations. Once the host initiates a programming or erasing operation, that operation will automatically continue to completion. The host does not need to intervene until the operation is finished. To check the status of the operation, poll status bit 6 of the instruction register.

operation (continued)

software sequence

The host initiates all of the SCOPE Diary's internal memory operations by issuing a sequence of address/data pairs (forming a specific software sequence) to the SCOPE Diary. The correct address/data pairs must be received in a specific order and within a specific time period to be recognized as a valid software sequence by the SCOPE Diary. Once a sequence has begun, the SCOPE Diary starts an internal sequence timer. Each consecutive address/data pair must be received within a 9 ms time period. After each address/data pair, the timer is reset to receive the next sequence pair. If the time between consecutive address/data pairs exceeds the timer limit, the internal state of the sequence detector will be reset, and the host must re-issue the software sequence from the beginning. If the SCOPE Diary detects a valid software sequence, status bit 5 of the instruction register will be set within 2 μs and will remain set as long as the SCOPE Diary is unlocked for the operation. The host may terminate a software sequence at any point by either letting the internal time limit expire, or by issuing a CLRSWS command. The software sequences recognized by the SCOPE Diary are shown in Table 7.

Table 7. SCOPE Diary Software Sequences

Operation	Address/Data Pair Sequence
Programming	5555h / AAh 2AAAh / 55h 5555h / A0h
Erasing	5555h / AAh 2AAAh / 55h 5555h / 80h 5555h / AAh 2AAAh / 55h 5555h / 10h
Program-Verify	5555h / AAh 2AAAh / 55h 5555h / B0h
Erase-Verify	5555h / AAh 2AAAh / 55h 5555h / D0h
Exit-Verify	5555h / AAh 2AAAh / 55h 5555h / F0h

page programming buffer

The page programming buffer is a 32-byte buffer that the host loads with the data to be programmed into the memory array. This buffer is internal to memory and can be accessed using the memory-address and memory-data registers. The page programming buffer is automatically selected by internal control logic after it detects a valid program software sequence. The contents of this buffer are automatically set to FFh, so any bits not specifically cleared by the host will not be programmed. Up to 32 bytes can be programmed in one cycle.

Address/data pairs must be loaded into the page programming buffer within the same time constraints as the software sequence. If the sequence timer is allowed to expire during a page programming buffer load, the internal control logic will terminate the programming operation and clear the software sequence detector (indicated by status bit 5 in the instruction register). During a programming operation, data that has been loaded into the internal page programming buffer is automatically transferred into the memory array.

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operation (continued)

operation initiation

The SCOPE Diary differs from typical software sequence-controlled memory devices because the selected programming or erasing operation does not automatically begin at the end of the internal sequence time out. To initiate the selected operation, the host must issue the BEGOPS command to the SCOPE Diary and enter the *Run-Test/Idle* state before the internal sequence timer expires. If the timer expires, the internal sequence detector will be cleared, and the selected operation must be re-initiated from the beginning. Status bit 6 in the instruction register indicates a successful program or erase operation. This bit will be set within 2 µs after the BEGOPS instruction is executed.

reset

The SCOPE Diary test bus logic is cleared either by internal circuitry at power-up, or by entry to the *Test-Logic-Reset* state. All internal data scan path registers are set to logic 0, and the instruction register is loaded with the IDCODE instruction. Entering the *Test-Logic-Reset* state will not clear a pending software sequence or interrupt an executing self-timed program or erase cycle.

erase-verify mode

The erase-verify mode allows the host to verify the adequacy of erasure. Once the SCOPE Diary has been placed in the verify mode, it will remain in that state (indicated in the instruction register when status bit 3 is a logical 1) until the exit-verify mode sequence has been issued. When in the erase-verify mode, the internal voltage applied to the read select lines (wordlines) is reduced by a preset margin. To verify that the array has been erased, the host reads the memory block and checks that all bits are set to logic 1.

program-verify mode

The program-verify mode allows the host to verify the adequacy of programming. Once the SCOPE Diary has been placed in the program-verify mode, it will remain in this state (indicated in the instruction register when status bit 3 is a logical 1) until the exit-verify mode sequence has been issued. When in the program-verify mode, the internal voltage applied to the read-select lines (wordlines) is increased by a preset margin. To verify that a programming operation was successful, the host reads the previously programmed locations and checks that the data values are correct.

JTAG extensions

DMA read

The DMA read mode allows any number of sequential bits to be read from the SCOPE Diary while remaining in the *Shift-DR* state. During a DMA read operation, the contents of the memory array will be shifted out beginning with the address location contained in the memory-address register. Upon entry to the *Shift-DR* state, an internal modulo 8 counter is triggered. This counter is used to increment the contents of the memory-address register on byte boundaries. After the data from the last byte in the memory array has been read, the next data will be read from the byte at the beginning of the memory array.

DMA write

The DMA write mode simplifies data transfer to the SCOPE Diary. This mode allows data to be continuously streamed into the SCOPE Diary while remaining in the *Shift-DR* state. Compared to normal modes of data transfer, the DMA write extensions enable systems with a large number of devices in the scan path to realize a significant reduction of clock cycles.

In the DMA write mode, an internal modulo 24 counter is used to automatically transfer address/data pairs to the memory core while bypassing the *Update-DR* state. To initiate a DMA write data transfer, the internal modulo 24 counter must be triggered (synchronized) when the first bit of an address/data pair is at the TDI input pin. The SCOPE Diary supports two methods of DMA synchronization: state-transition mode and header mode. The host determines which method of DMA synchronization is used.

ADVANCE INFORMATION

JTAG extensions (continued)

state-transition mode

The host selects state-transition mode by clearing the header register (all bits to logic 0). When the state-transition mode is selected, incoming scan path data is ignored during first entry to the *Shift-DR* state. The first entry to *Pause-DR* indicates proper alignment at the TDI input pin of the first address/data pair. Re-entry to the *Shift-DR* state triggers the modulo 24 counter and enables the address/data pair to be written to the memory core. Address/data pairs can then be streamed continuously to the SCOPE Diary with internal transfers occurring automatically on 24-bit boundaries.

header mode

The host selects the header mode by loading the header register with a value from 01h to FFh. When the header mode is selected, incoming scan path data is ignored until a byte (matching the contents of the header register) arrives indicating the arrival of valid address/data pairs. When this header byte is detected, the internal modulo 24 counter is triggered. Address/data pairs can then be streamed continuously to the SCOPE Diary with internal transfers occurring automatically on 24-bit boundaries.

In either state-transition or header mode, the host places the SCOPE Diary in the *Update-DR* state to end a DMA write operation. Because placing the SCOPE Diary in the *Update-DR* state ends the operation, the host must *never* place the SCOPE Diary in this state until the DMA write operation is complete. The host may place the SCOPE Diary in the *Pause-DR* state at any time.

operation examples

Note that in this section, the letter “n” denotes a value from 0h to Fh, and the letter “x” denotes a don’t care.

reading examples

reading using the byte mode

Step 1. Load the BYTERD instruction.
Step 2. Scan in 16-bit address = *nnnn* and 8-bit data = *xx.*
Step 3. Scan out 16-bit address = *nnnn* and 8-bit data = *nn.*

reading using the DMA mode

Step 1. Load the LDADDR instruction.
Step 2. Scan in 16-bit address = *nnnn.*
Step 3. Load the DMARD instruction.
Step 4. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values, the address register is automatically incremented on byte boundaries.

lockbit examples

reading lockbits using the byte mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the BYTERD instruction.
Step 3. Scan in 16-bit address = 0000 and 8-bit data = *xx.*
Step 4. Scan out 16-bit address = 0000 and 8-bit data = F*n.*
Step 5. Load the CLRLOCK instruction.

reading lockbits using the DMA mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the DMARD instruction.
Step 3. Scan out the 8-bit lock value = F*n.*
Step 4. Load the CLRLOCK instruction.

ADVANCE INFORMATION

operation examples (continued)

programming lockbits using the byte mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the BYTEWR instruction.
Step 3. Scan in address = 5555 and data = AA, go to *Run-Test/Idle.*
Step 4. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 5. Scan in address 5555 and data = A0; go to *Run-Test/Idle.*
Step 6. Scan in address = 0000, and data = F*n*; go to *Run-Test/Idle.*
Step 7. Load the BEGOPS instruction; go to *Run-Test/Idle.*
Step 8. Load the CLRLOCK instruction.

programming lockbits using the DMA mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the DMAWR instruction.
Step 3. Synchronize SCOPE Diary using either state-transition mode or header mode.
Step 4. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 5. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 6. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 7. Continue looping in *Shift-DR* to scan in address = 0000 and data = F*n*.
Step 8. Load the BEGOPS instruction; go to *Run-Test/Idle.*
Step 9. Load the CLRLOCK instruction.

flash erase examples

erasing a block using the byte mode

Step 1. Load the ERABLK instruction.
Step 2. Scan in the 4-bit erase-block-select value = *n*.
Step 3. Load the BYTEWR instruction.
Step 4. Scan in address = 5555 and data = AA; go to *Run-Test/Idle.*
Step 5. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 6. Scan in address = 5555 and data = 80; go to *Run-Test/Idle.*
Step 7. Scan in address = 5555 and data = AA; go to *Run-Test/Idle.*
Step 8. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 9. Scan in address = 5555 and data = 10; go to *Run-Test/Idle.*
Step 10. Poll the SCOPE Diary until valid sequence is detected.
Step 11. Load the BEGOPS instruction; go to *Run-Test/Idle.*

erasing a block using the DMA mode

Step 1. Load the ERABLK instruction.
Step 2. Scan in the 4-bit erase-block-select value = *n*.
Step 3. Load the DMAWR instruction.
Step 4. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 5. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 6. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 7. Continue looping in *Shift-DR* to scan in address = 5555 and data = 80.
Step 8. Continue looping in *Shift-DR* to scan in address = 5555 and data = AA.
Step 9. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 10. Continue looping in *Shift-DR* to scan in address = 5555 and data = 10.
Step 11. Poll SCOPE Diary until valid sequence is detected.
Step 12. Load the BEGOPS instruction; go to *Run-Test/Idle.*

ADVANCE INFORMATION

operation examples (continued)

verifying block erasure using the byte mode

select the erase-verify mode:

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle.*
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 4. Scan in address = 5555 and data = D0; go to *Run-Test/Idle.*

read out the erased block:

Step 5. Load the BYTERD instruction.
Step 6. Scan in 16-bit address = *nnnn* and 8-bit data = *xx.*
Step 7. Scan out 16-bit address = *nnnn* and 8-bit data = FF; at the same time, scan in 16-bit address = *nnnn*+1 and data = *xx*.
Step 8. Repeat Step 7 until entire block is read. All bits will be a logic 1 if the block is properly erased.

exit the erase-verify mode:

Step 9. Load the BYTEWR instruction.
Step 10. Scan in address = 5555 and data = AA; go to *Run-Test/Idle.*
Step 11. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 12. Scan in address = 5555 and data = F0; go to *Run-Test/Idle.*

verifying block erasure using the DMA mode

select the erase-verify mode:

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = D0.

read out the erased block:

Step 6. Load the LDADDR instruction.
Step 7. Scan in 16-bit data starting address = *nnnn* of the block you want to verify.
Step 8. Load the DMARD instruction.
Step 9. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values from the addressed block. All bits will be a logic 1 if the block is properly erased.

exit the erase-verify mode:

Step 10. Load the DMAWR instruction.
Step 11. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 12. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 13. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 14. Continue looping in *Shift-DR* to scan in address = 5555 and data = F0.

verifying programming using the byte mode

select the program-verify mode:

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle.*
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 4. Scan in address = 5555 and data = B0; go to *Run-Test/Idle.*

read out the programmed data:

Step 5. Load the BYTERD instruction.
Step 6. Scan in 16-bit address = *nnnn* and 8-bit data = *xx.*
Step 7. Scan out 16-bit address = *nnnn* + 1 and 8-bit data = *nn*; at the same time, scan in 16-bit address=*nnnn* + 1 and data = *xx*.
Step 8. Repeat Step 7 until desired memory locations are read and verified.

operation examples (continued)

exit the program-verify mode

Step 9. Load the BYTEWR instruction.
Step 10. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 11. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 12. Scan in address = 5555 and data = F0; go to *Run-Test/Idle*.

verifying programming using the DMA mode

select the program-verify mode:

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = B0.

read out the programmed data:

Step 6. Load the LDADDR instruction.
Step 7. Scan in 16-bit starting address = *nnnn* of the data you want to verify.
Step 8. Load the DMARD instruction.
Step 9. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values starting from the addressed location. Verify that the output data stream matches the programmed data.

exit the program-verify mode:

Step 10. Load the DMAWR instruction.
Step 11. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 12. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 13. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 14. Continue looping in *Shift-DR* to scan in address = 5555 and data = F0.

programming examples

programming a single byte using the byte mode

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 4. Scan in address = 5555 and data = A0; go to *Run-Test/Idle*.
Step 5. Scan in address = *nnnn* and data = *nn*; go to *Run-Test/Idle*.
Step 6. Load the BEGOPS instruction; go to *Run-Test/Idle*.

programming a single byte using the DMA mode

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 6. Continue looping in *Shift-DR* to scan in address = *nnnn* and data = *nn*.
Step 7. Load the BEGOPS instruction; go to *Run-Test/Idle*.

programming a page using the byte mode

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 4. Scan in address = 5555 and data = A0; go to *Run-Test/Idle*.
Step 5. Scan in address = *nnnn* and data = *nn*; go to *Run-Test/Idle*.
Step 6. Go to Step 5 while there are address/data pairs to load within the 32-byte page.
Step 7. Load the BEGOPS instruction, go to *Run-Test/Idle*.

ADVANCE INFORMATION

operation examples (continued)

programming a page using the DMA mode

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 6. Continue looping in *Shift-DR* to scan in address = *nnnn* and data = *nn*.
Step 7. Go to Step 6 while there are address/data pairs to load within the 32-byte page.
Step 8. Load the BEGOPS instruction; go to *Run-Test/Idle*..

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 3) .... – 0.6 V to 7 V
Input voltage range: All except DLA (see Note 3) .... – 0.6 V to 6.5V
Input voltage range: DLA (see Note 3) .... – 0.6 V to 15 V
Output voltage (see Note 3) .... – 0.6 V to V_{CC} + 0.6V
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... – 65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: Voltage values are with respect to GND (substrate).

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	TTL	2		V_{CC} + 1	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level input voltage	TTL	– 0.5		0.8	V
		CMOS	GND – 0.2		GND + 0.2	
T_A	Operating free-air temperature		0		70	°C
Endurance cycles					1000	
Programming operations					100 000	

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.0 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)	DLA, DLB	V_I = 2.4 V		+ 75	+ 150	µA
		DLA, DLB	V_I = 0 V			± 10	
		TDI, TMS	V_I = 0.4		– 10	– 50	
		TDI, TMS	V_I = V_{CC} = 5.5 V			± 10	
I_O	Output current (leakage)		V_O = 0.1 to V_{CC}			± 10	µA
I_{CC1}	V_{CC} average supply current (active read)		t_{cycle} = 160 ns, outputs open			20	mA
I_{CC2}	V_{CC} average supply current (active write)		t_{cycle} = 15 ms			15	mA

‡ Typical values are at T_A = 25° and nominal voltages.

ADVANCE INFORMATION

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_I	Input capacitance	$V_I = 0$, f = 1 MHz		4	7	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		8	12	pF

† Capacitance measurements are made on sample basis only
‡ Typical values are at $T_A = 25°C$ and nominal voltage.

switching characteristics over full ranges of recommended operating conditions

PARAMETER		MIN	MAX	UNIT
t_{DA}	TDO valid from falling edge of TCK		74	ns
t_{DZ}	TDO disable time from falling edge of TCK		35	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_{CYC}	TCK cycle time	160		ns
$t_{W(TCKH)}$	Pulse duration, TCK high	50		ns
$t_{W(TCKL)}$	Pulse duration, TCK low	70		ns
$t_{SU(TMS)}$	TMS input setup time	15		ns
$t_{IH(TMS)}$	TMS input hold time	5		ns
$t_{SU(TDI)}$	TDI input setup time	6		ns
$t_{IH(TDI)}$	TDI input hold time	15		ns

internal timing requirements

PARAMETER		MIN	MAX	UNIT
t_{SSS}	Software sequence status bit valid from software sequence		2	µs
t_{PEBS}	Program erase busy status bit valid from BEGOPS execution		2	µs
t_{ST}	Sequence timer limit		9	ms

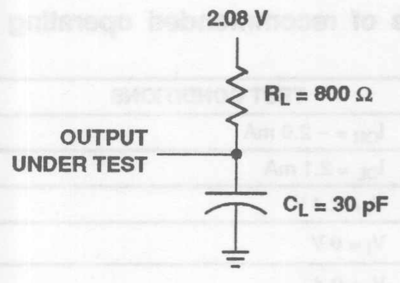
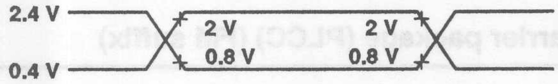


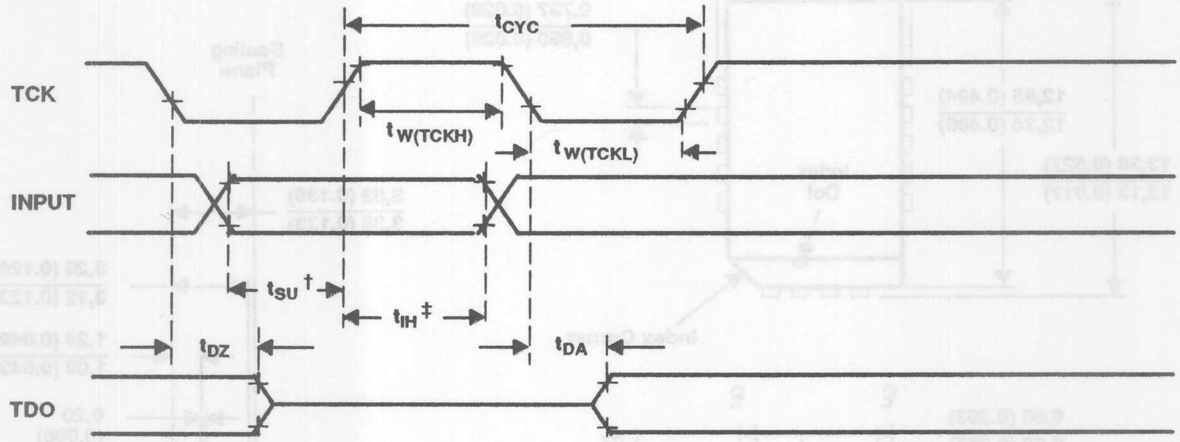
Figure 5. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 for logic low. Timing measurements are made at 2 V for logic 1 and 0.8 V for both inputs and outputs. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and GND as close as possible to the device pins.

timing diagram

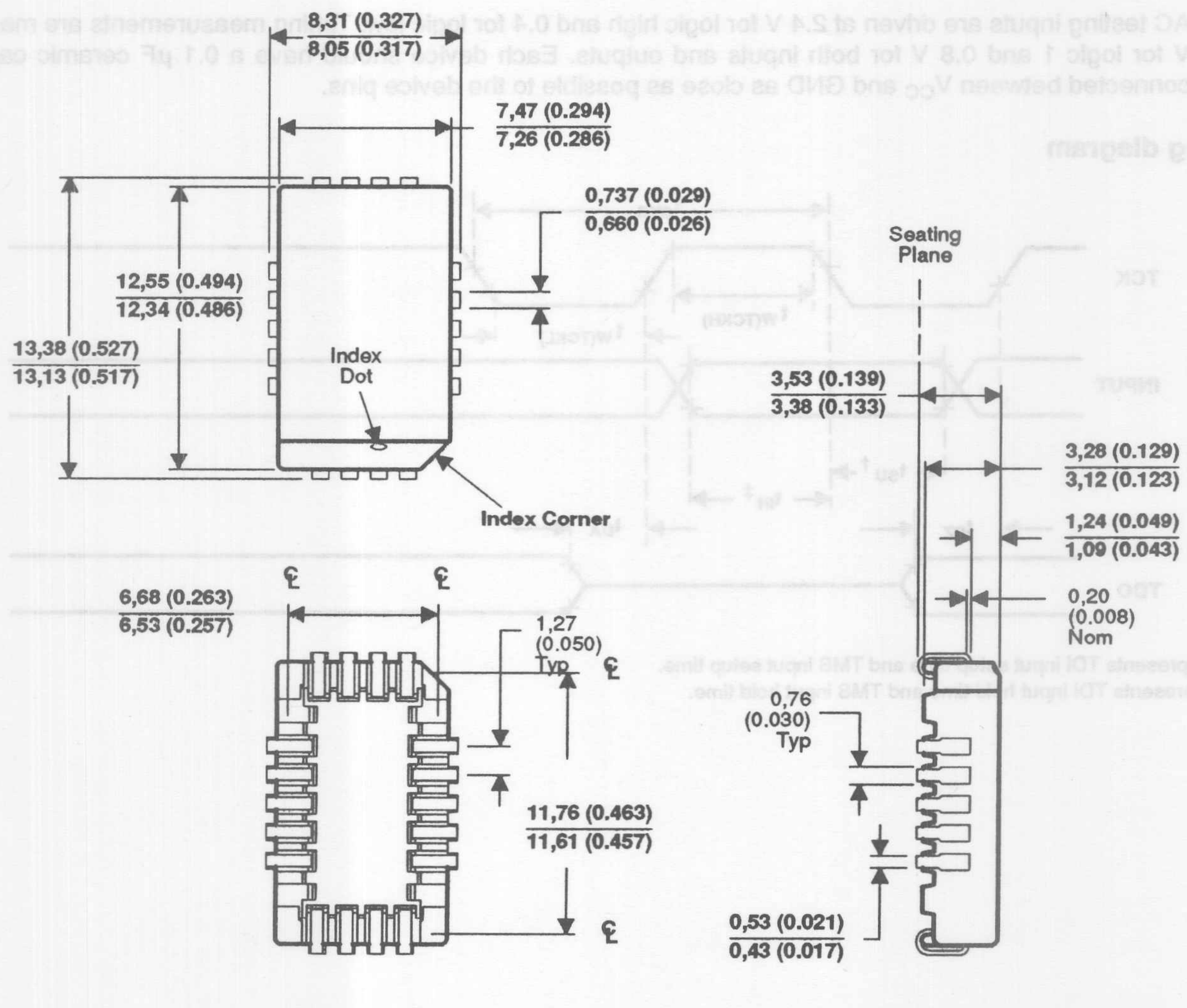


† t_{SU} represents TDI input setup time and TMS input setup time.
‡ t_{IH} represents TDI input hold time and TMS input hold time.

ADVANCE INFORMATION

MECHANICAL DATA

18-pin plastic leaded-chip carrier package (PLCC) (FM suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

JTAG Data Sheets 1

Customer Presentation 2

U.S. GENERAL PURPOSE LOGIC
SCOPE TESTABILITY PRODUCTS

Design Support Matrix

DEVICE	DESCRIPTION	BSDL	BERKLEY I/O SPICE MODEL	LMI BEHAVIORAL MODEL	QUAD DESIGN MODEL
BCT8240A	Octal Driver	Y	–	Y	TBD
BCT8244	Octal Buffer	Y	–	Y	TBD
BCT8245A	Octal Transceiver	Y	Y	Y	TBD
BCT8373	Octal Latch	Y	–	Y	TBD
BCT8374	Octal Flip-Flop	Y	–	Y	TBD
ABT8245	Octal Transceiver	Y	4Q92	4Q92	TBD
ABT8543	Registered Transceiver With Latch	Y	4Q92	4Q92	TBD
ABT8646	Registered Transceiver	Y	4Q92	4Q92	TBD
ABT8652	Enhanced Registered Transceiver	Y	4Q92	4Q92	TBD
ABT8952	Registered Transceiver With Clock Enable	Y	4Q92	4Q92	TBD
ABT18245	18-bit Transceiver	4Q92	4Q92	4Q92	TBD
ABT18502	20-bit Universal Bus Transceiver	Y	Y	Y	TBD
ABT18504	18-bit Universal Bus Transceiver	Y	Y	Y	TBD
ABT18646	18-bit Registered Transceiver	4Q92	Y	4Q92	TBD
ABT18652	18-bit Registered Transceiver	4Q92	Y	4Q92	TBD
ACT8990	Test Bus Controller	–	–	Y	–
ACT8994	Digital Bus Monitor	Y	–	Y	–
ACT8997	Scan Path Linker	TBD	–	Y	–
ACT8999	Scan Path Selector	TBD	–	Y	–
TMS29F816	Diary Memory	Y	–	TBD	–

SCOPE™

Widebus+™

SCOPE WIDEBUS +
NEW PRODUCT PROPOSAL

KEY QUESTIONS

IS THERE A GENERAL NEED FOR THIS PRODUCT ?

DO YOU AGREE WITH OUR PROPOSED ARCHITECTURE ?

WHAT FUNCTIONS ARE MOST DESIRABLE ?

WHEN WOULD THIS PART NEED TO BE AVAILABLE ?

HOW MUCH VALUE DO YOU PERCEIVE THIS PRODUCT HAS FOR YOU ?

ADVANCED BiCMOS TECHNOLOGY (ABT)

SCOPE™ Products

- High-performance, low power 0.8 µ BiCMOS.
- Wide acceptance in telecom, workstation and high-end computer systems.
- Max T_{pd}

	ABT646	ABT8646
Max T_{pd}	5.4 ns	5.5 ns

- Five SCOPE Octal devices (SOIC, SSOP) available now, four planned.
- New 24/28 SSOP packaging (less than half the size of SOIC) also available.
- Eight SCOPE Widebus devices (SQFP , SSOP) planned.
- New Widebus+™ (32/36-bit functions) parts being considered in 100- or 120-pin SQFP.

ABT38XXX

Features

- 32- and 36-bit bus interface functions.
- Packaged in 100- and 120-pin SQFP (Shrink Quad Flat Package).
- High-performance EPIC-IIB process (0.8 µm CMOS and bipolar).

SCOPE™ Widebus+™

Feature		***Benefit***
• EPIC-IIB	→	Save valuable board space
• Shrink Quad Flat Pack (0.5 mm lead-pitch)	→	Advance BiCMOS technology
• Wide architectures 32- and 36-bit wide	→	Reduces package count, board space and manufacturing cost *
• Bipolar outputs $I_{OL} = 64$ mA $I_{OH} = -32$ mA	→	High drive capability
• High speed $T_{pd} < 4$ ns (typ)	→	Increase system performance
• Low noise < 0.8 V SS noise Distributed V_{CC}/GND	→	High signal integrity
• Bus hold circuitry	→	Holds unused or floating inputs at a valid logic state
• -40°C to 85°C	→	Extended temperature range

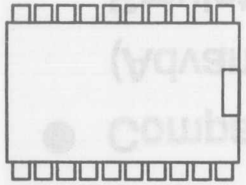
* Reduces overhead of four additional JTAG pins

SCOPE™ Widebus+™

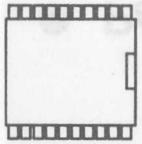
Feature		Benefit
• Compatible with JTAG/IEEE 1149.1 - 1990 test standard	→	Implements industry-standard boundary scan techniques that support fault isolation to the component level
• Part of TIs SCOPE family of testability products	→	Provides a complete line of products dedicated to solving testability problems
• Compatible with TIs ASSET™ (Advanced Support System for Emulation and Test) software	→	Simplifies design debugging and hardware testing

ADVANCED BUS INTERFACE PACKAGING SOLUTIONS

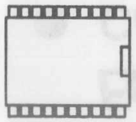
8-Bits



20-Pin SOIC (DW)
Area = 137 mm^2
Height = 2.65 mm
Lead Pitch = 1.27 mm

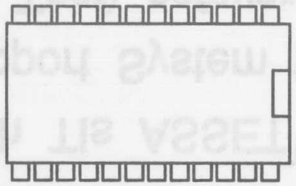


20-Pin SSOP (DB)
Area = 62 mm^2
Height = 2.0 mm
Lead Pitch = 0.65 mm

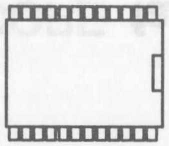


20-Pin TSSOP (PW)
Area = 46 mm^2
Height = 1.1 mm
Lead Pitch = 0.65 mm

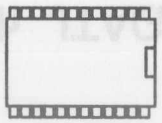
8/9-Bits



24-Pin SOIC (DW)
Area = 165 mm^2
Height = 2.65 mm
Lead Pitch = 1.27 mm



24-Pin SSOP (DB)
Area = 70 mm^2
Height = 2.0 mm
Lead Pitch = 0.65 mm



24-Pin TSSOP (PW)
Area = 54 mm^2
Height = 1.1 mm
Lead Pitch = 0.65 mm

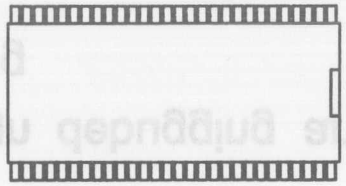
16/18-Bits

Widebus™

48-Pin SSOP (DL)
Area = 171 mm^2
Height = 2.74 mm
Lead Pitch = 0.635 mm

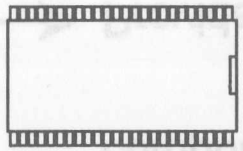
16/18-Bits

Widebus™

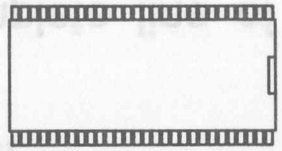


56-Pin SSOP (DL)
Area = 198 mm^2
Height = 2.74 mm
Lead Pitch = 0.635 mm

New Shrink-Widebus™



48-Pin TSSOP (DGG)
Area = 108 mm^2
Height = 1.1 mm
Lead Pitch = 0.5 mm



56-Pin TSSOP (DGG)
Area = 120 mm^2
Height = 1.1 mm
Lead Pitch = 0.5 mm

100-Pin SQFP (PZ)
Area = 266 mm^2
Height = 1.5 mm
Lead Pitch = 0.5 mm

120-Pin Heat Spreader SQFP (PCB)
Area = 266 mm^2
Height = 2.3 mm
Lead Pitch = 0.4 mm

(TI package designators)

Widebus, Shrink-Widebus, and Widebus+ are trademarks of Texas Instruments Incorporated.

SCOPE™ Widebus+™

ABT – Advanced BiCMOS Technology

- **Functionally equivalent to popular bus interface devices in normal mode.**

- **Bus width of 36 bits accommodates bus transfers with parity.**

- **Nomenclature: SN 74 ABT 38 600 PCB**

74	**series:** 74 = commercial series, 54 = military series
ABT	**technology:** ABT = 0.8 micron BiCMOS
38	**pinout:** 38 = IEEE 1149.1-1990 (JTAG) compatible Widebus+
600	**FAST-equivalent function type:** 600 = registered bus transceiver
PCB	**package:** PCB = 120-pin C-SQFP (cavity shrink quad flat pack)

- **Proposed function types:**

'ABT38245	non-inverting transceiver with direction control
'ABT38543	transceiver with in-line D-type latches
'ABT38600	transceiver with in-line D-type latches and D-type flip-flops
'ABT38646	transceiver with D-type flip-flops and real/stored data mux
'ABT38902	parity transceiver with in-line D-type latches and D-type flip-flops
'ABT38952	transceiver with in-line D-type flip-flops and clock enable

SCOPE™ Widebus+™

ABT – Advanced BiCMOS Technology

- **Compatible with IEEE Standard 1149.1-1990 (JTAG) serial test bus.**
- **Support IEEE Standard 1149.1-1990 instructions:**
  Required: EXTEST, SAMPLE/PRELOAD, BYPASS
  Optional: IDCODE

★ **EXTEST External Test**
capture external input data; source external output data for board level interconnect and functional test

★ **SAMPLE/PRELOAD**
capture external input data; capture outputs of internal logic for non-intrusive data sampling

★ **BYPASS**
select Bypass register for minimum scan delay

★ **IDCODE Identification Code**
select Device Identification register for identification of manufacturer, function type, and version

SCOPE™ Widebus+™

ABT – Advanced BiCMOS Technology

- **Compatible with IEEE Standard 1149.1-1990 (JTAG) serial test bus.**

- **Support proposed IEEE Standard 1149.1A instructions: HIGHZ, CLAMP**

  ★ **HIGHZ Control Outputs to High-Impedance**
  force outputs to high-impedance state
  Bypass register selected for minimum scan delay

  ★ **CLAMP Control Outputs to 1/0**
  source external output data from boundary-scan register
  Bypass register selected for minimum scan delay

SCOPE™ Widebus+™

ABT – Advanced BiCMOS Technology

- **Compatible with IEEE Standard 1149.1-1990 (JTAG) serial test bus.**
- **Support extended instruction set for Built-In-Self-Test (BIST):**
  CELLTST, READBN, READBT, TOGGLE/HOLD, TOGGLE/SAMPLE TOGGLE/PSA, PRPG/PSA, COUNT/PSA

★ **CELLTST** **Boundary Self Test**
capture complement of boundary cell for self test

★ **READBN** **Read Boundary Normal Mode**
READBT **Read Boundary Test Mode**
capture current contents of boundary cell for non-destructive read out

★ **TOGGLE/HOLD** **Toggle Outputs/Hold Inputs**

★ **TOGGLE/SAMPLE** **Toggle Outputs/Sample Inputs**

★ **TOGGLE/PSA** **Toggle Outputs/Parallel Signature Analysis**

★ **PRPG/PSA** **Pseudo-Random Pattern Generation/Parallel Signature Analysis**

★ **COUNT/PSA** **Count Up/Parallel Signature Analysis**

SCOPE™ Widebus+™

Built-In-Self-Test (BIST) Features

- **BIST features provide facilities for board-level built-in self-test**

- **BIST features provide several algorithms for signal capture/analysis at inputs**

  ★ **HOLD**
  inputs are held at a fixed logic level.

  ★ **SAMPLE**
  inputs are sampled in each TCK cycle during Run-Test/Idle state.

  ★ **PSA** **Parallel Signature Analysis**
  inputs are sampled in each TCK cycle during Run-Test/Idle state and are compressed to a 36-bit signature according to a linear feedback shift algorithm.

SCOPE™ Widebus+™

Built-In-Self-Test (BIST) Features

- **BIST features provide facilities for board-level built-in self-test**

- **BIST features provide several algorithms for pattern generation at outputs**

  ⋆ **TOGGLE**
  outputs are toggled in each TCK cycle during Run-Test/Idle state.

  ⋆ **PRPG** **Pseudo-Random Pattern Generation**
  outputs are changed in each TCK cycle during Run-Test/Idle state according to a 36-bit pseudo-random linear feedback shift algorithm.

  ⋆ **COUNT** **Binary Count**
  outputs are changed in each TCK cycle during Run-Test/Idle state according to a 36-bit binary count up algorithm.

SCOPE™ Widebus+™

Feature Comparison

Feature	ABT			BCT
	Wb+	Wb	Octal	Octal
IEEE Std 1149.1 instructions:				
Required EXTEST, SAMPLE/PRELOAD, BYPASS	✓	✓	✓	✓
Optional INTEST		✓	✓	✓
Optional IDCODE	✓	✓		
1149.1A Optional HIGHZ, CLAMP	✓	✓	✓	✓
SCOPE™ extensions for BIST:				
CELLTST, READBN, READBT	✓	✓	✓	✓
TOGGLE/HOLD, TOGGLE/SAMPLE, PRPG/PSA	✓	✓	✓	✓
COUNT/PSA	✓	✓	✓	
TOGGLE/PSA	✓			
PSA input masking		✓	✓	

SCOPE™ Widebus+™

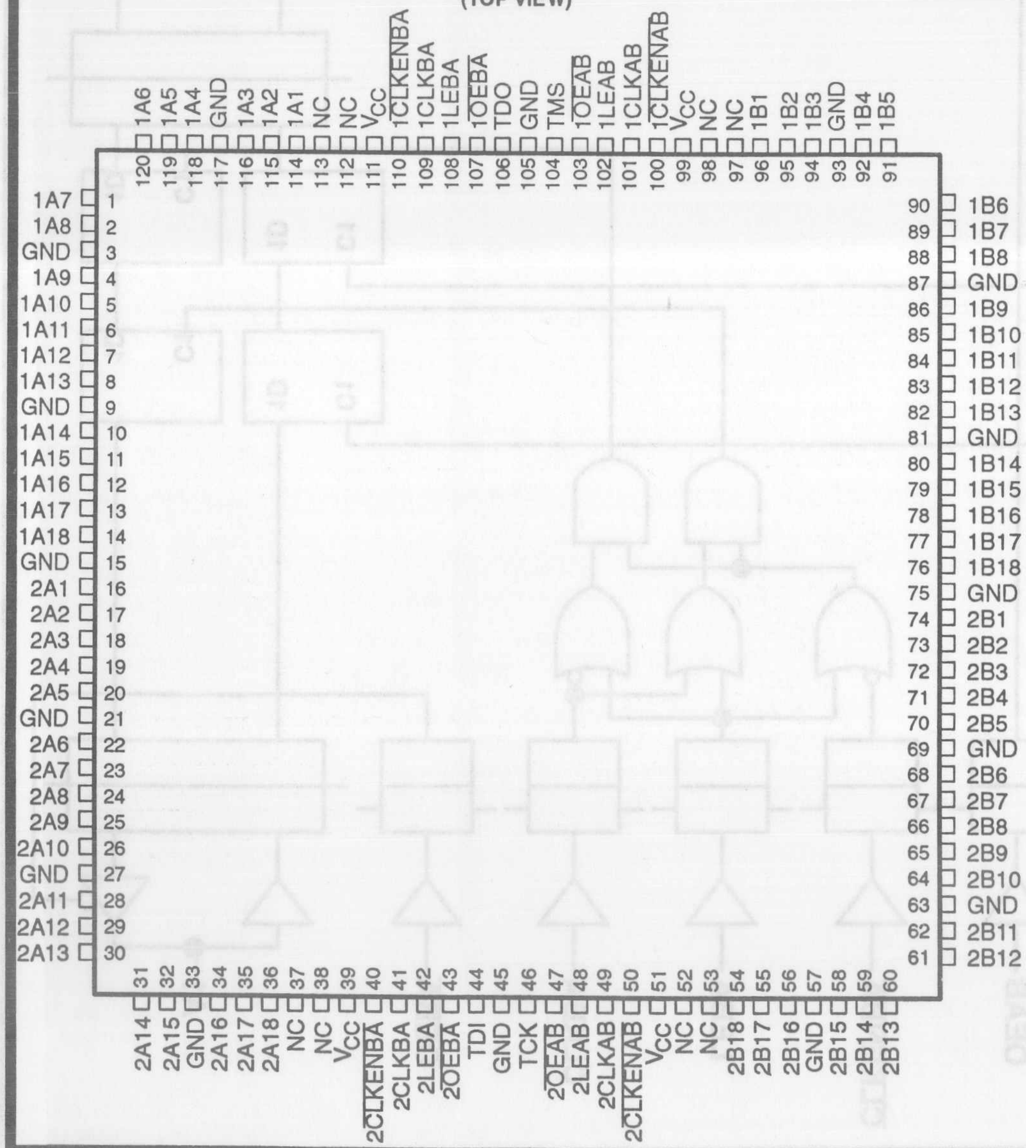
Feature Comparison

Feature	ABT			BCT
	Wb+	Wb	Octal	Octal
Other features:				
Even–parity instruction opcodes	✓	✓	✓	
Indirect BIST instructions (Boundary Control Register)		✓	✓	✓
Direct BIST instructions (No Boundary Control Register)	✓			
Dual boundary scan cells for I/O ports		✓	✓	
Merged boundary scan cells for I/O ports	✓			
Bus–hold circuit at inputs	✓			

SCOPE™ Widebus+™

ABT38600

SN74ABT38600...PCB PACKAGE
(TOP VIEW)



- **Unique control logic allows data transfer in transparent, latched, and clocked modes.**
- **Control logic is replicated for 2 banks of 18 channels for 2x18 or 1x36 data transfers.**
- **Can substitute for a multitude of function types:**

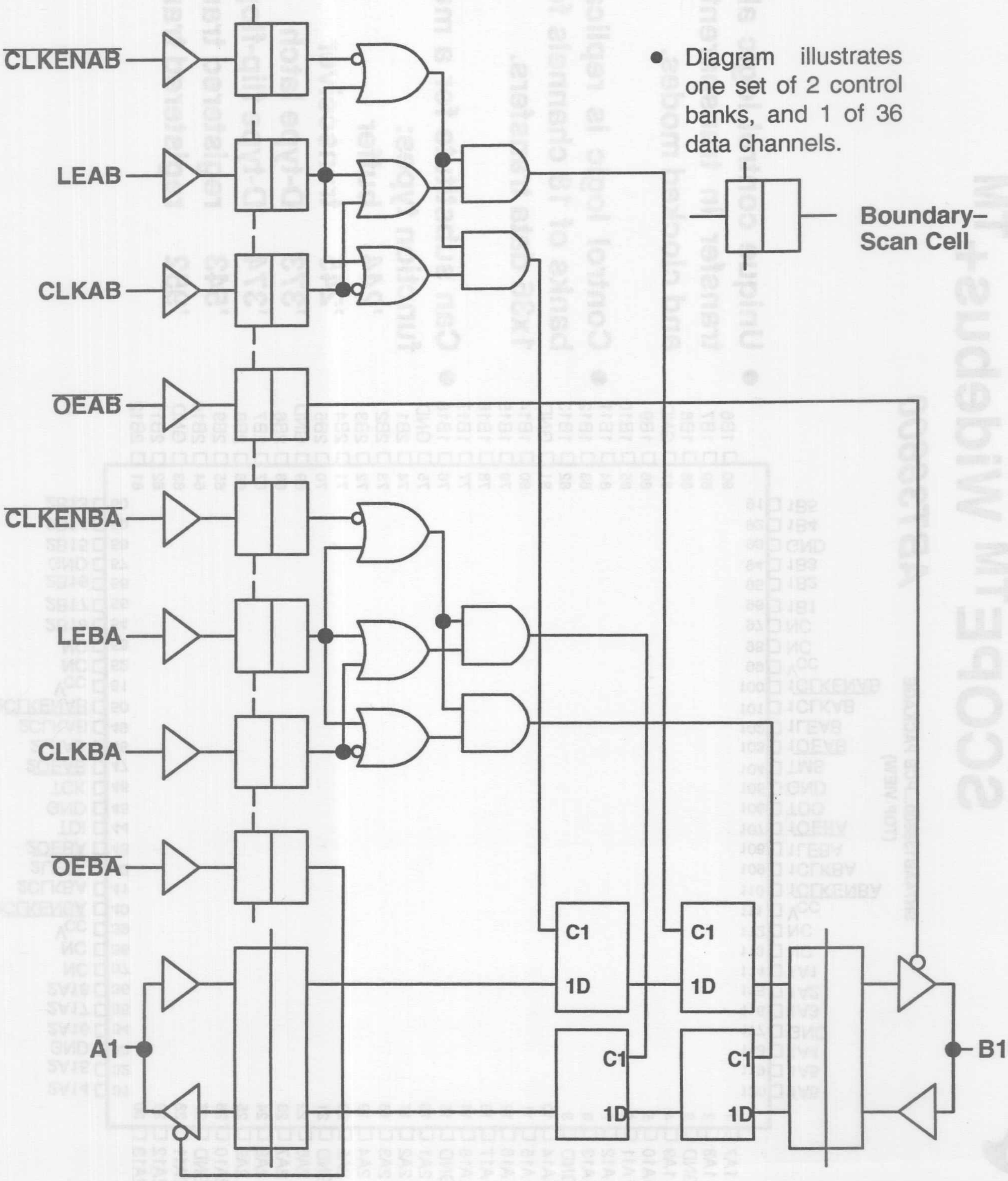
'244	buffer
'245	transceiver
'373	D-type latch
'374	D-type flip-flop
'543	registered transceiver
'952	registered transceiver

SCOPE™ Widebus+™

ABT38600

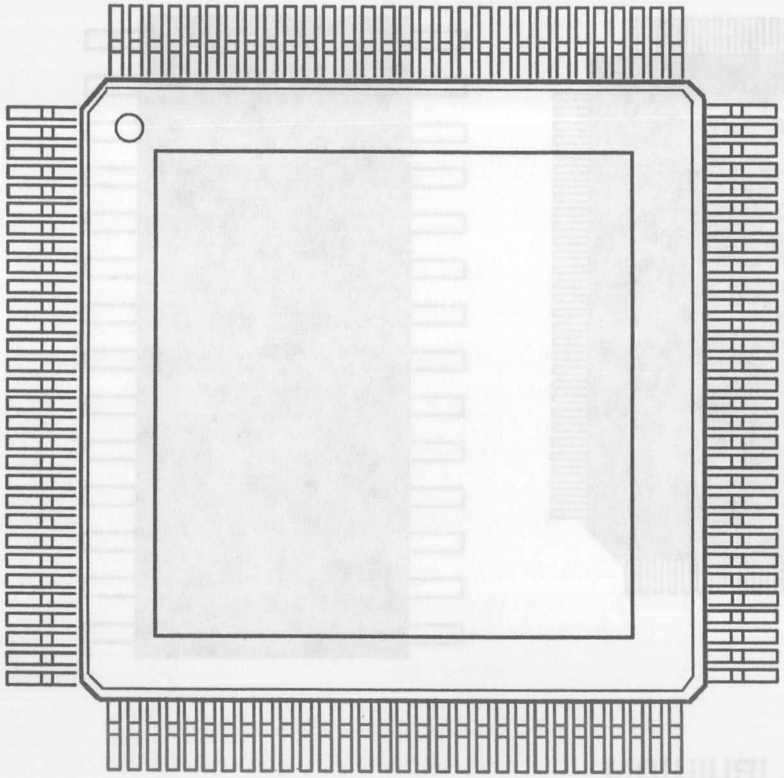
Functional Block Diagram

- Diagram illustrates one set of 2 control banks, and 1 of 36 data channels.



SCOPE™ Widebus+™

C-SQFP – 120-pin Cavity Shrink Quad Flat Pack

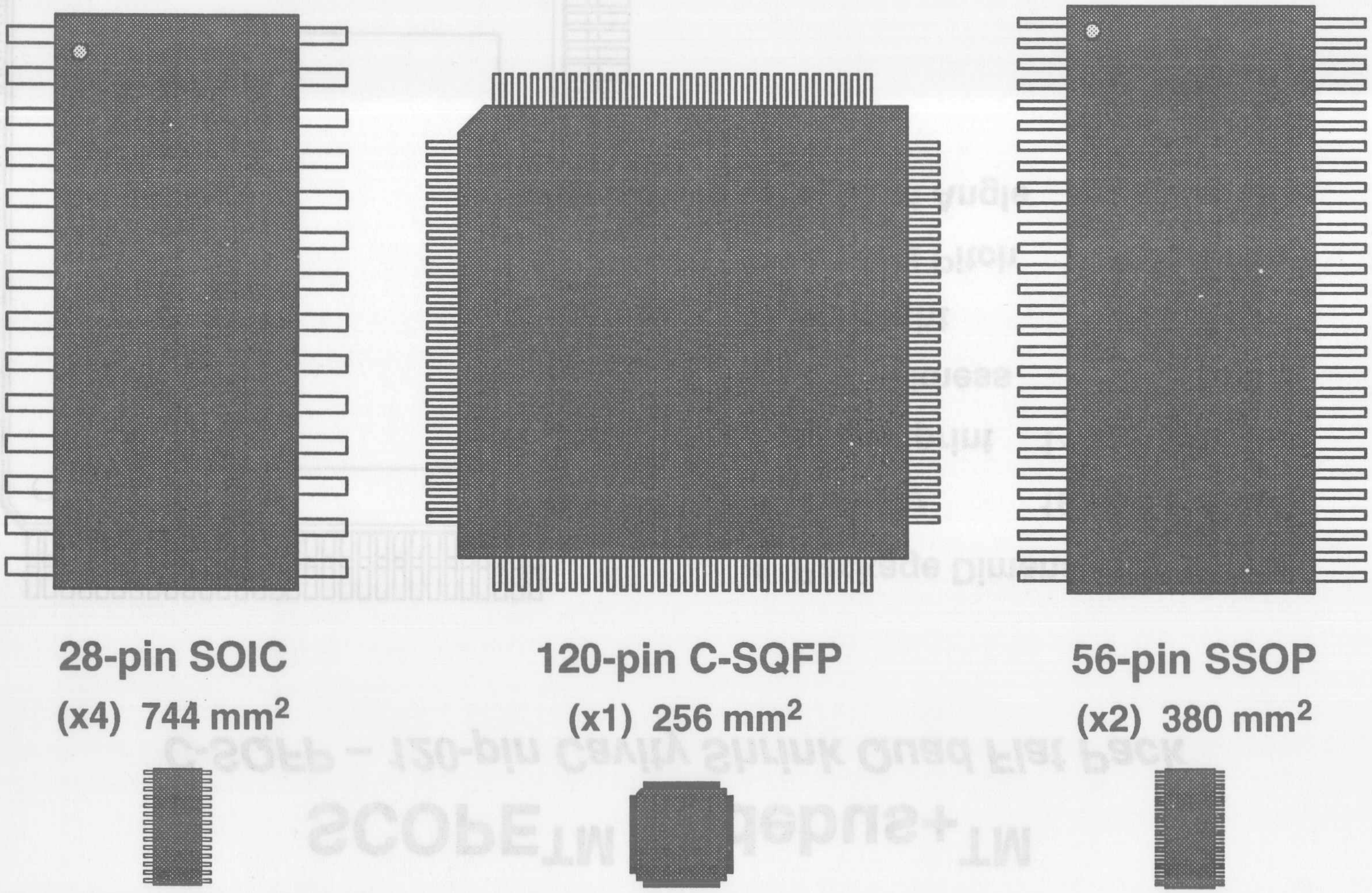


- **Package Dimensions**
  - ★ **Body** 16 mm x 16 mm
  - ★ **Footprint** 14 mm x 14 mm
  - ★ **Thickness** 2.1 mm
  - ★ **Height** 2.3 mm
  - ★ **Lead Pitch** 0.4 mm
  - ★ **Lead Angle** 2°

SCOPE™ Widebus+™

Package Comparison

Nominal Footprint Area



SCOPE™ Widebus+™

Package Comparison

C-SQFP versus SSOP and SOIC

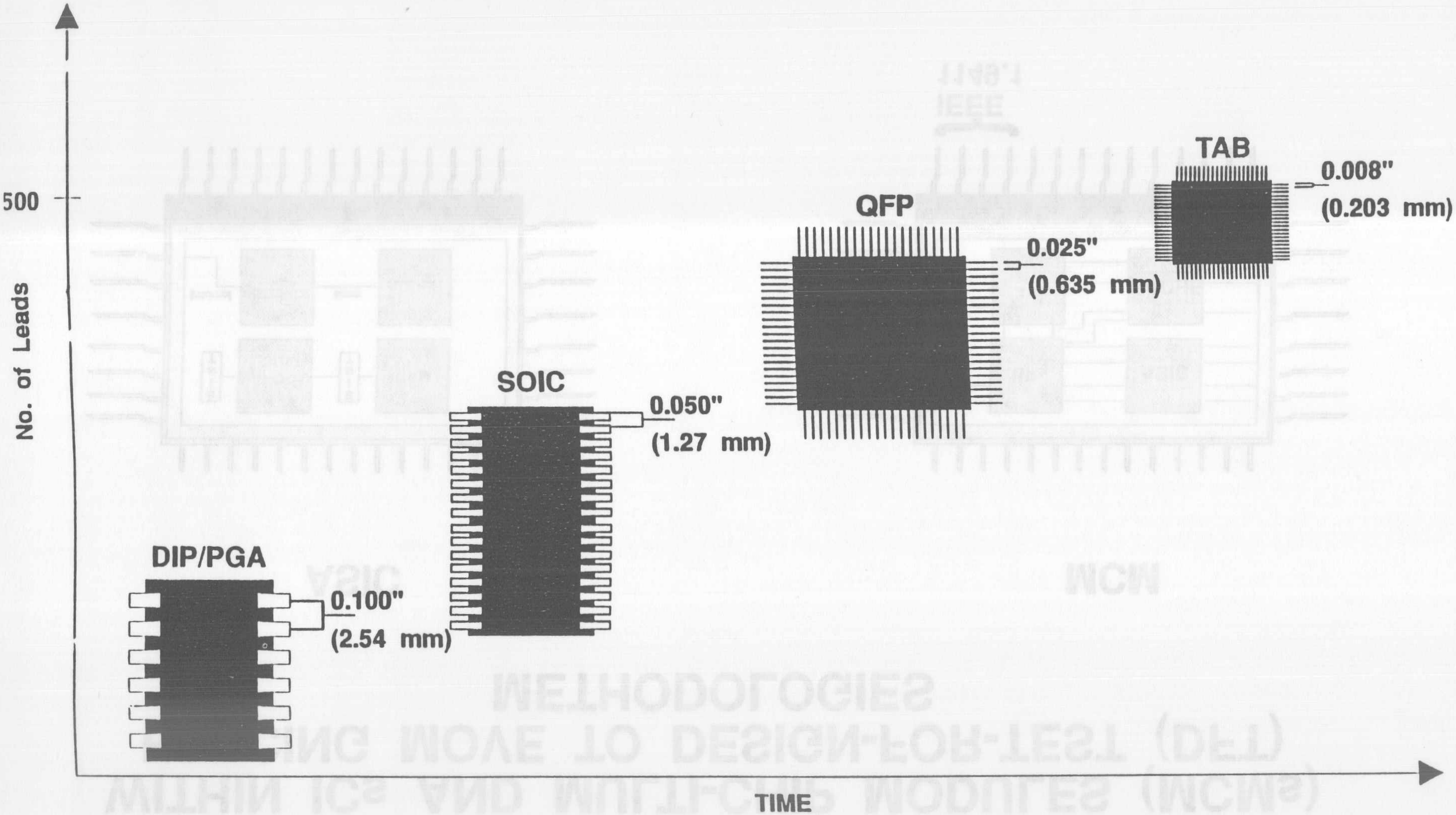
(all dimensions in mm unless otherwise noted)

Physical dimension	SQFP	SSOP	SOIC
Nominal Body Size	14 X 14	7.5 X 18.4	6.6 X 17.9
Nominal Body Area (mm^2)	196	138	119
Nominal Footprint Size	16 X 16	10.5 X 18.4	10.4 X 17.9
Nominal Footprint Area (mm^2)	256	190	186
Maximum Height	2.3	2.74	2.65
Nominal Lead Pitch	0.4	0.635	1.27
Nominal Lead Width	0.2	0.25	0.44
Nominal Lead Spacing	0.2	0.385	0.83

ASSET v2.0

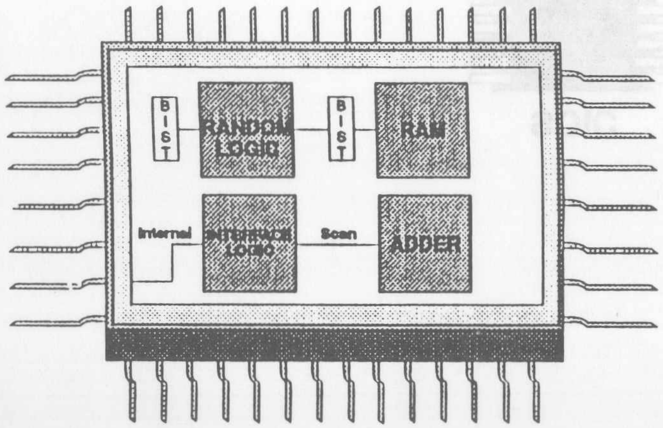
CUSTOMER PRESENTATION

Packaging Density is Increasing Dramatically . . .

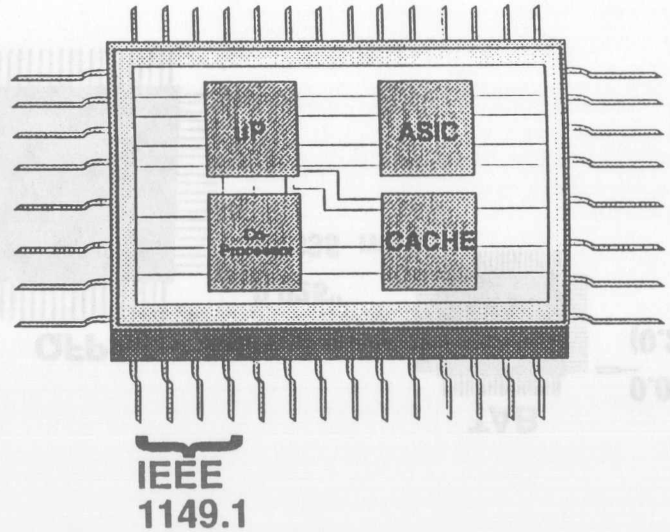


INCREASING FUNCTIONAL DENSITY WITHIN ICs AND MULTI-CHIP MODULES (MCMs) FORCING MOVE TO DESIGN-FOR-TEST (DFT) METHODOLOGIES

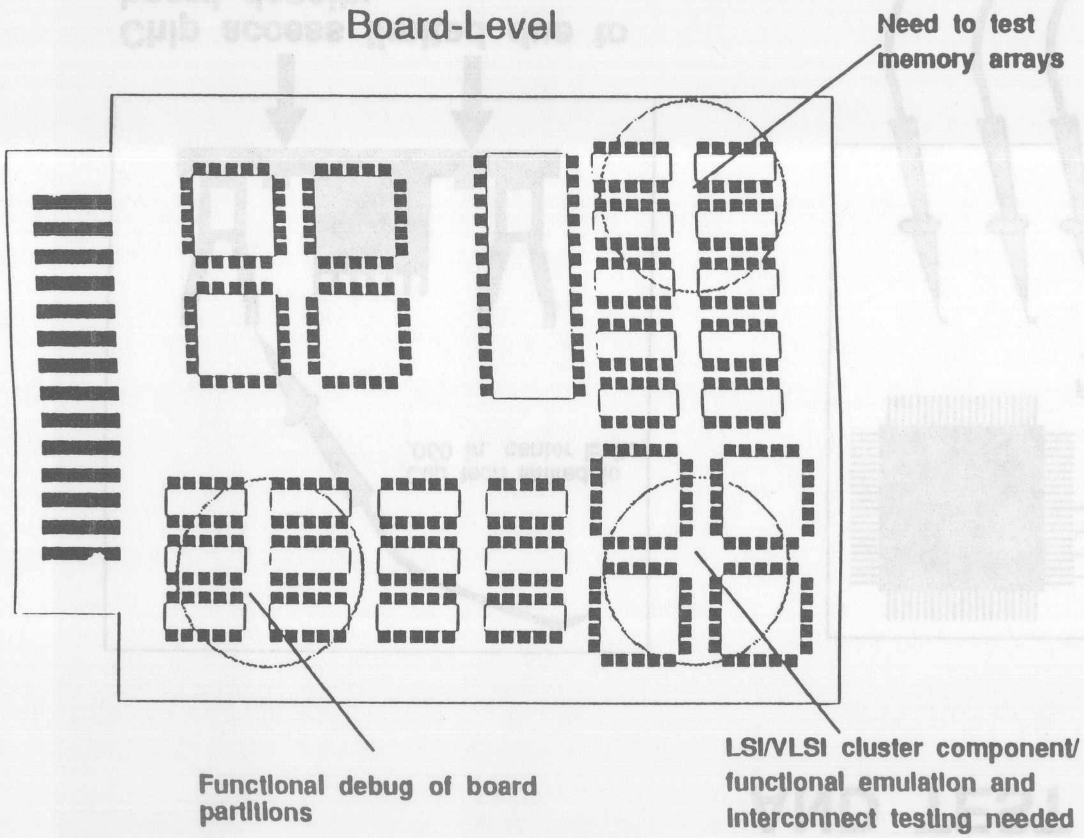
ASIC

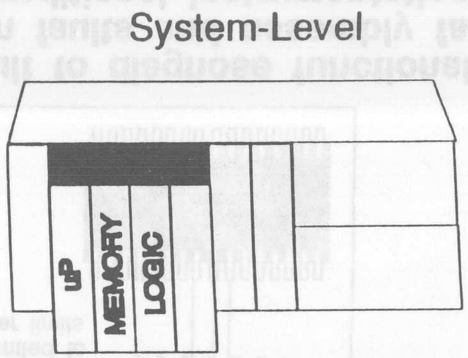


MCM



INCREASED FUNCTIONAL DENSITY AT THE BOARD AND SYSTEM LEVEL ARE MAKING DEBUG AND INTEGRATION MORE DIFFICULT

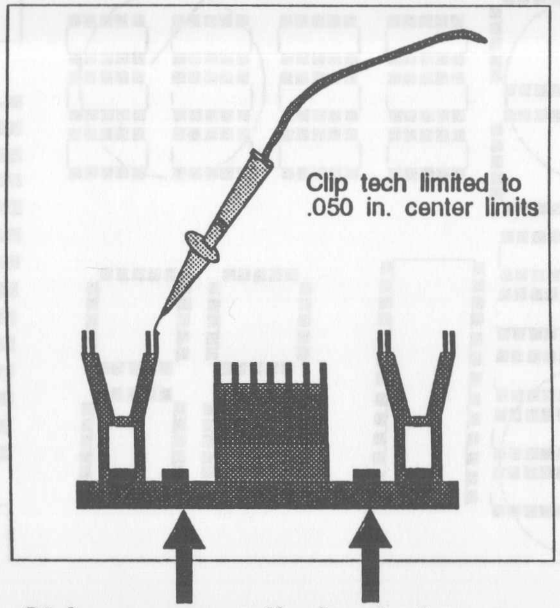




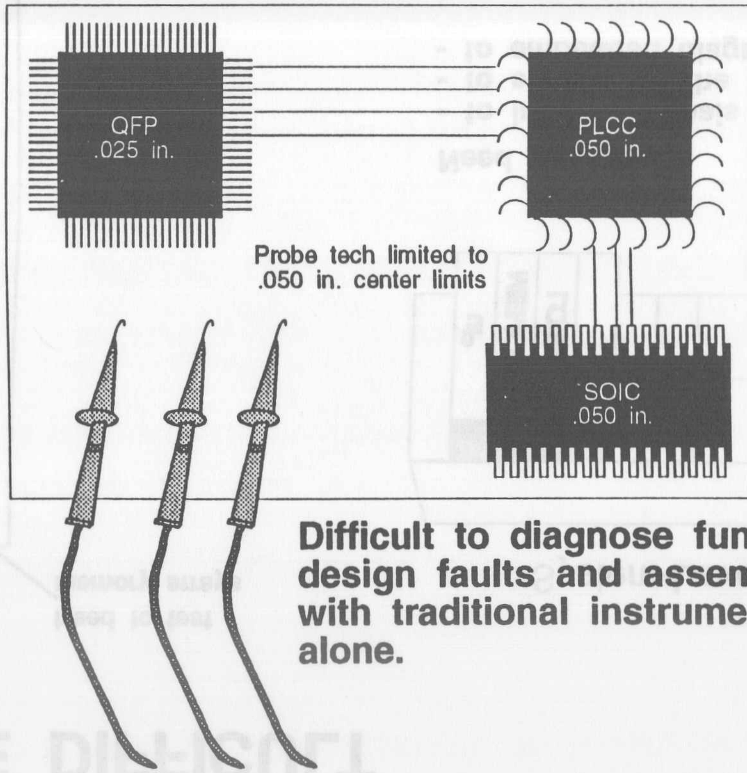
Need Access

- to internal signals
- to signals on the backplane
- to embedded diagnostic software

HIGH DENSITY/SMT PACKAGING IS REMOVING PHYSICAL ACCESS FOR DOING DESIGN VERIFICATION AND TEST

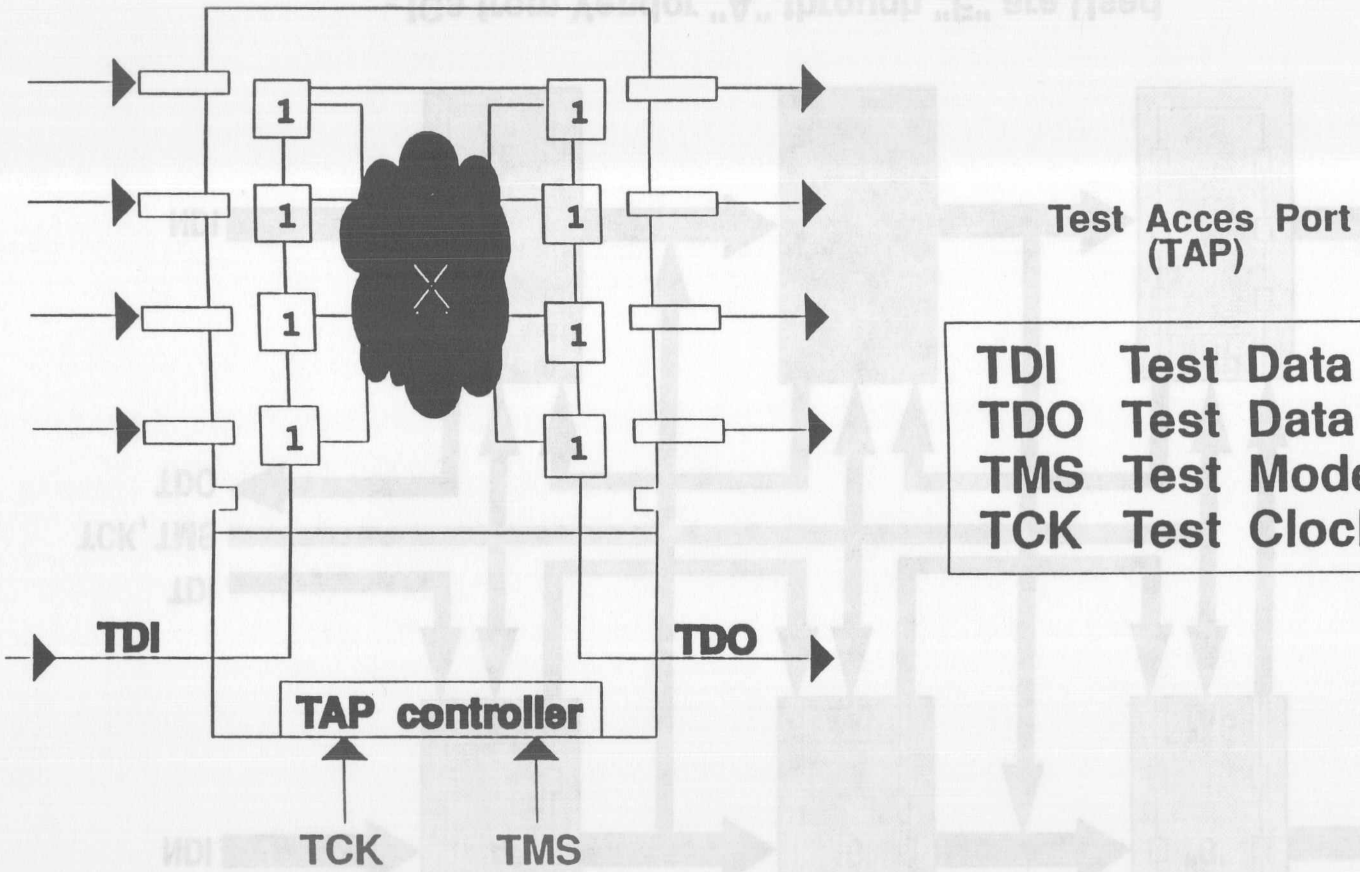


Chip access limited due to board density



Difficult to diagnose functional design faults and assembly faults with traditional instrumentation alone.

THE IEEE STD. 1149.1-1990 PROVIDES "VIRTUAL" ACCESS AND CONTROL



TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
TCK	Test Clock

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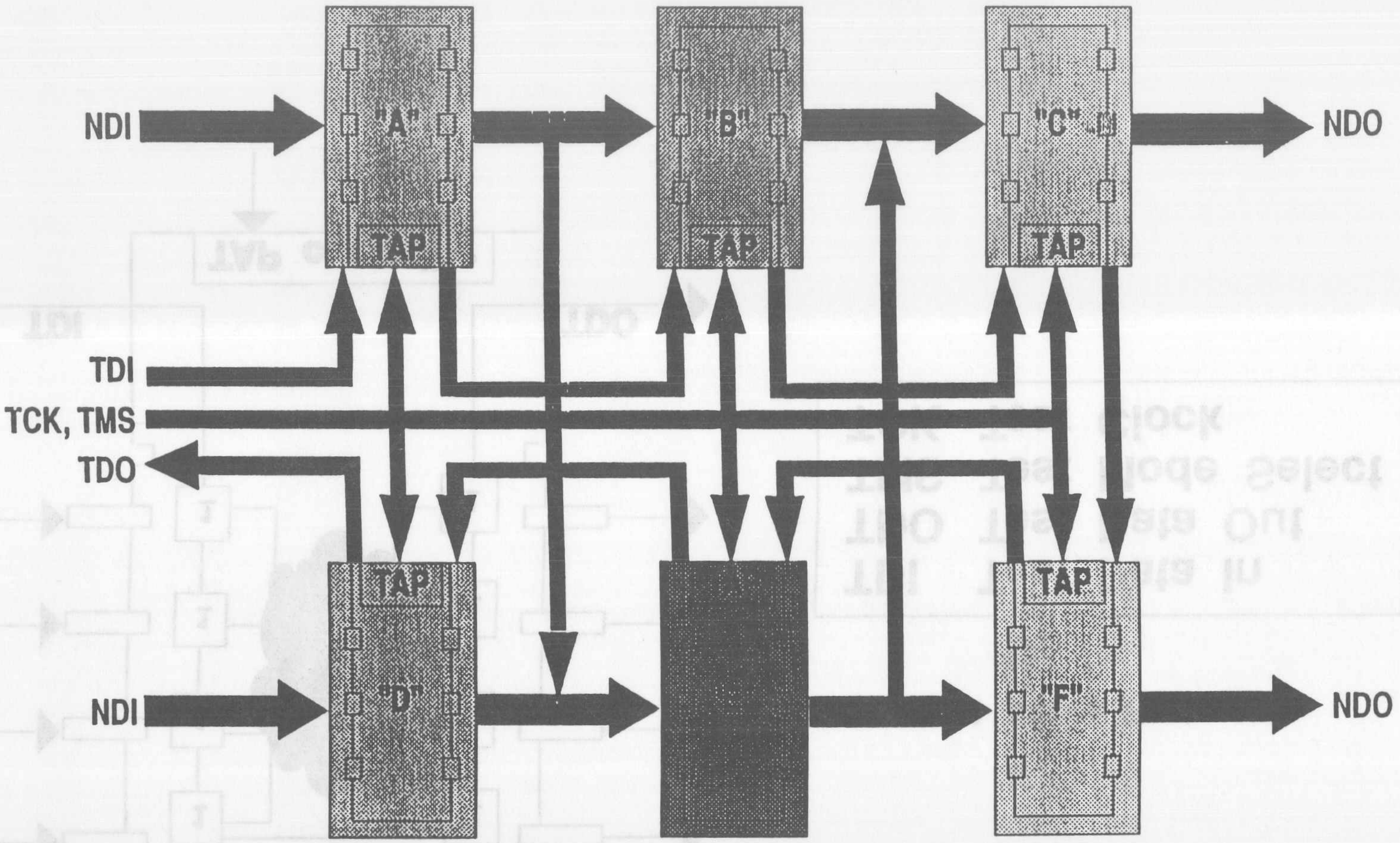
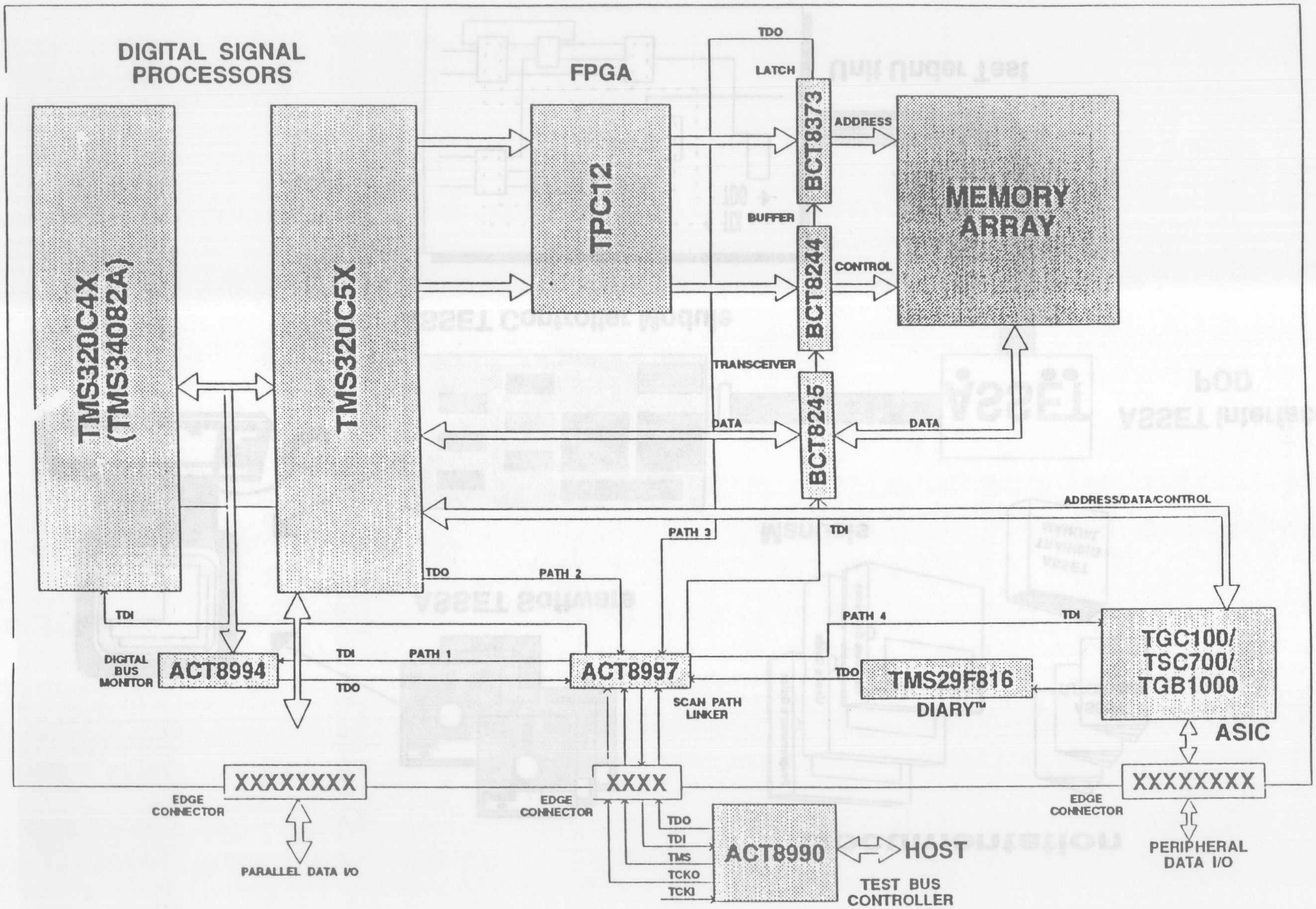
CIRCUIT INCORPORATING JTAG STANDARD

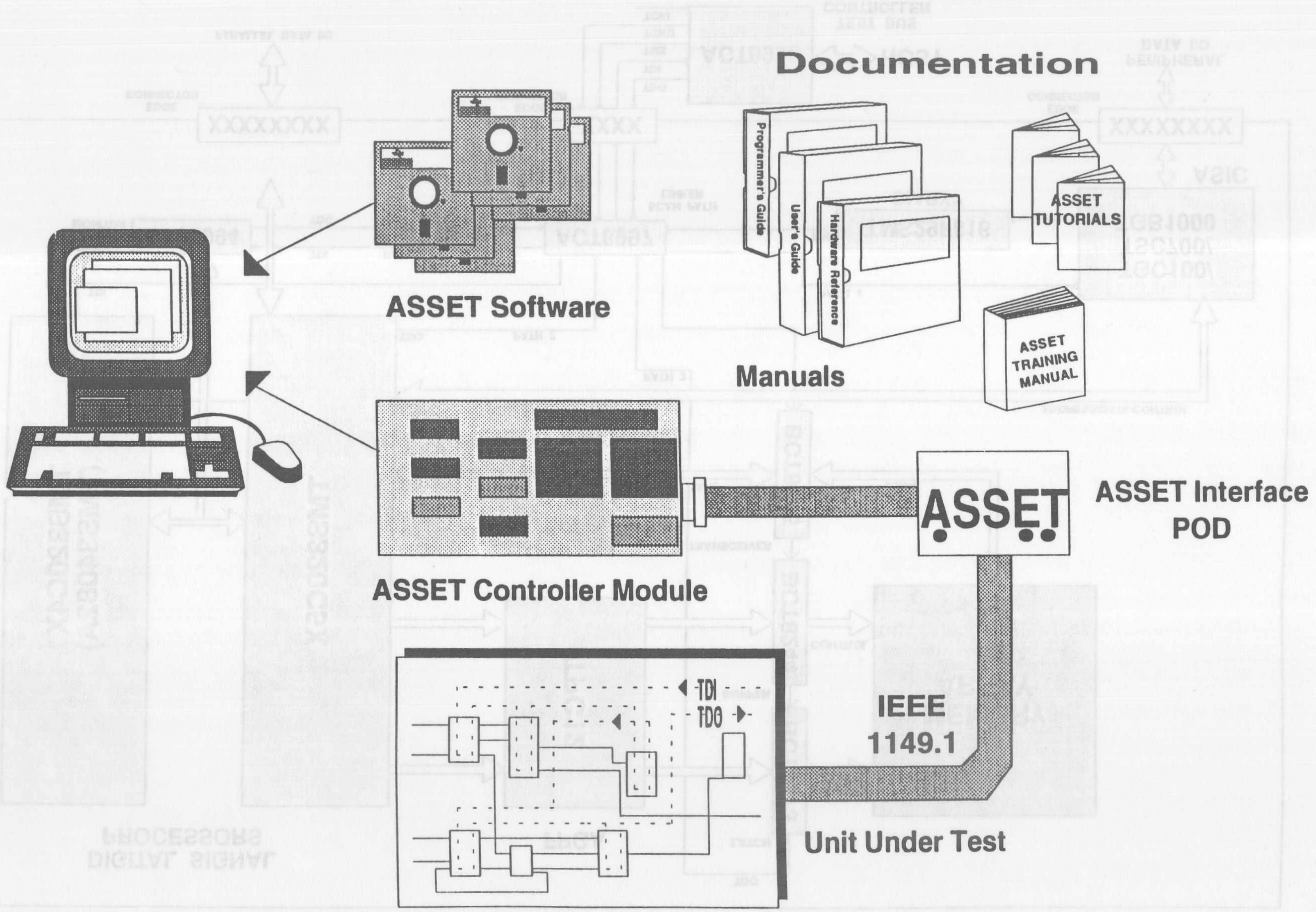


- ICs from Vendor "A" through "F" are Used
- All ICs Include JTAG Boundary Scan and Tap
- Wiring Interconnects Between ICs are Easily Tested
- Vendors May Include Buildt-In Self Test In ICs "A"-"F"

TI SCOPE SILICON PRODUCTS



ASSET DIAGNOSTIC SYSTEM



ASSET 2.0: ADDRESSES DESIGN VERIFICATION CUSTOMER CARE-ABOUTS

- Easy-to-Use
  - Logical, human understandable representations of the scan path
  - Interactive debug supporting pin, register, and bus control
  - Macros simplify test vector and program development
  - Mouse-driven U/I - MS Windows 3.1
- Hierarchical Design Description Support for System Debug
  - HSDL
  - Hierarchical interactive viewing
  - BIST and internal scan supported
- Analysis Features Like a Logic Analyzer
  - Waveform and State Table display supported
  - Triggering and Sequencing supported
- Go/No Go Batch Test Applications
  - SVF Input/Output
  - CAE Parallel Vector Serialization

ASSET 2.0: ADDRESSES DESIGN VERIFICATION CUSTOMER CARE-ABOUTS

- 100% B.S. Interconnect ATPG and Fault Diagnostics
  - ASSET/VICTORY Integration
- Standards Supported
  - SVF, BSDL, HSDL, EDIF
- Embedded Test Application Support for System Integration
  - Scan Engine
- Flow to Embedded
  - ASSET ⇨ SVF ⇨ Scan Engine
- C/C++ Test Program Development Supported
  - Scan Function Library Supports Microsoft, Borland, and Zortech C/C++ Compiler
- More Care-Abouts
- " " "

R & D LAB - DIAGNOSTIC TOOL NEEDS OF THE 90's

Traditional Hardware/ Software Debug

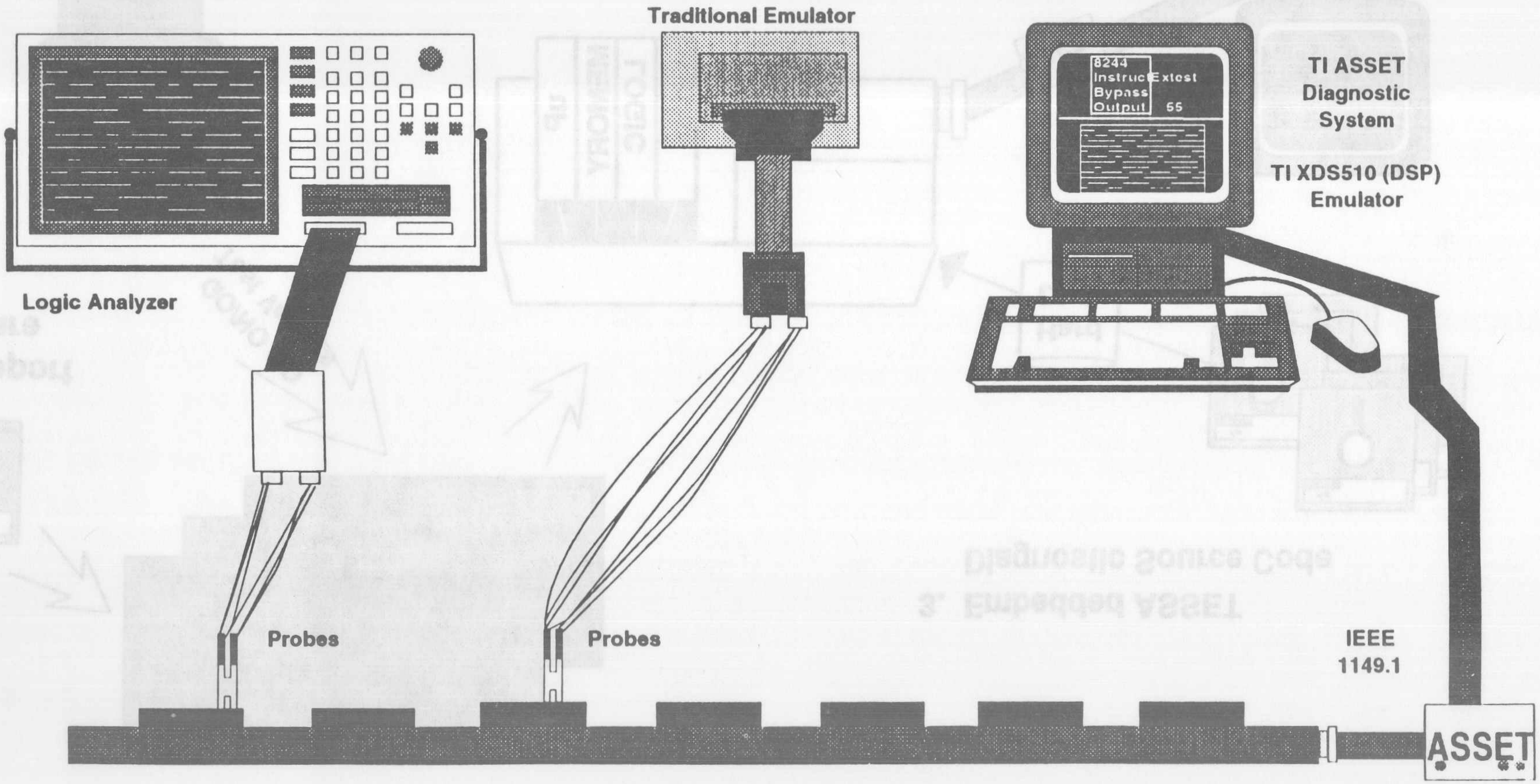
- Hardware Timing
- Hardware Functionality
- Software Analysis

Traditional Software Debug

- Application Program Development/Debug

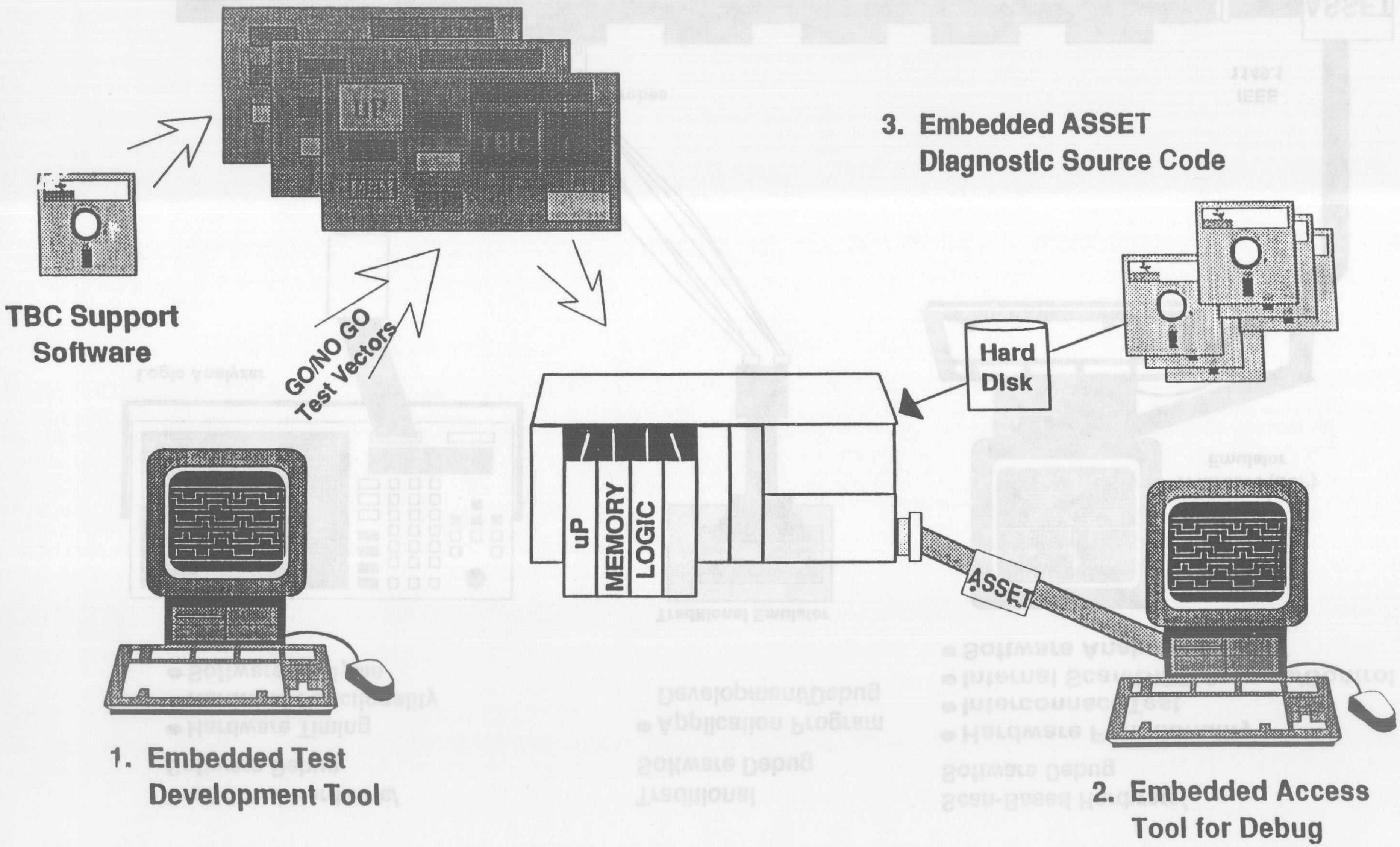
Scan-Based Hardware/ Software Debug

- Hardware Functionality
- Interconnect Test
- Internal Scan/BIST Access/Control
- Software Analysis

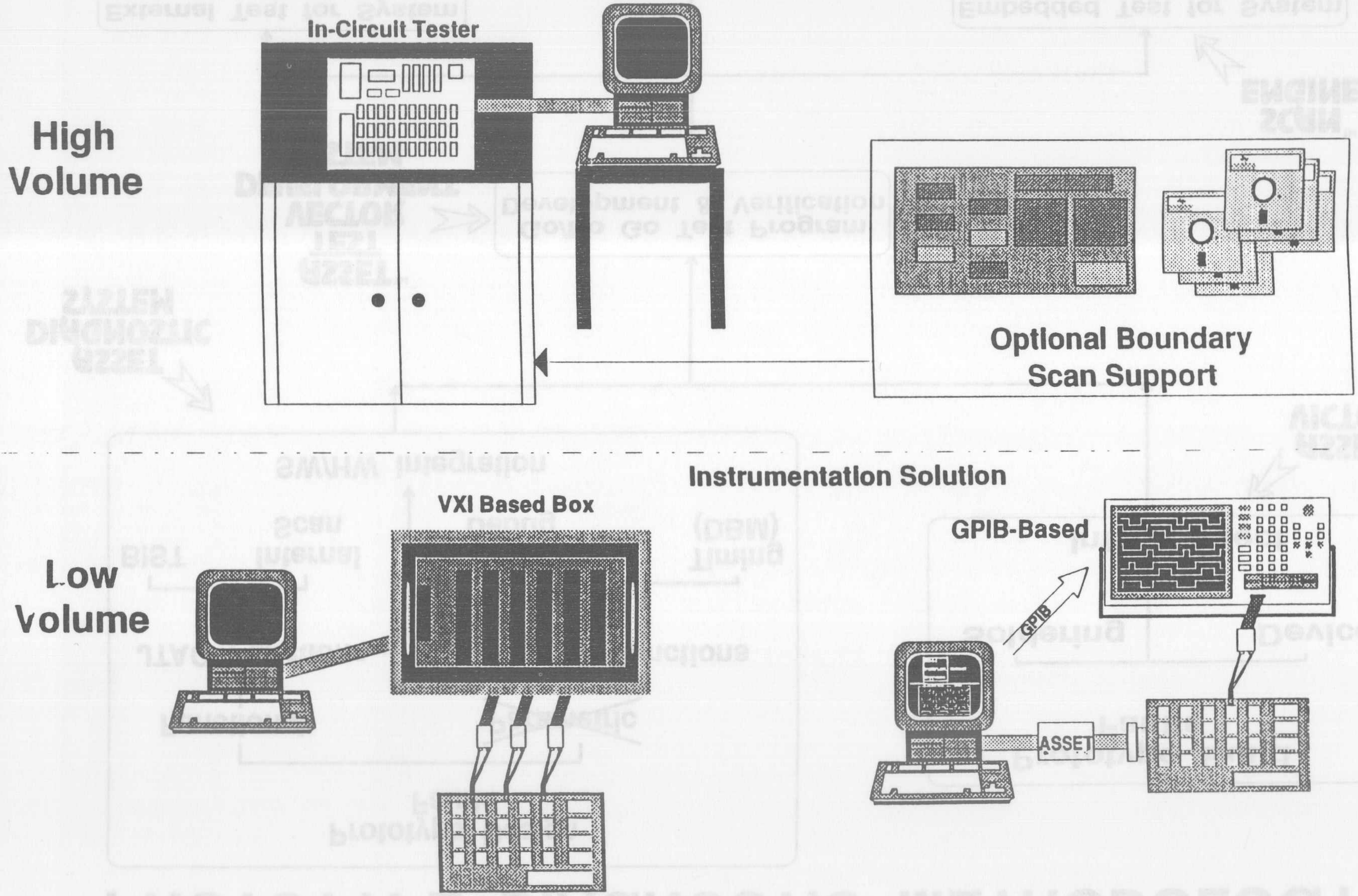


Mixed Boundary Scan/ Non-Boundary Scan Boards

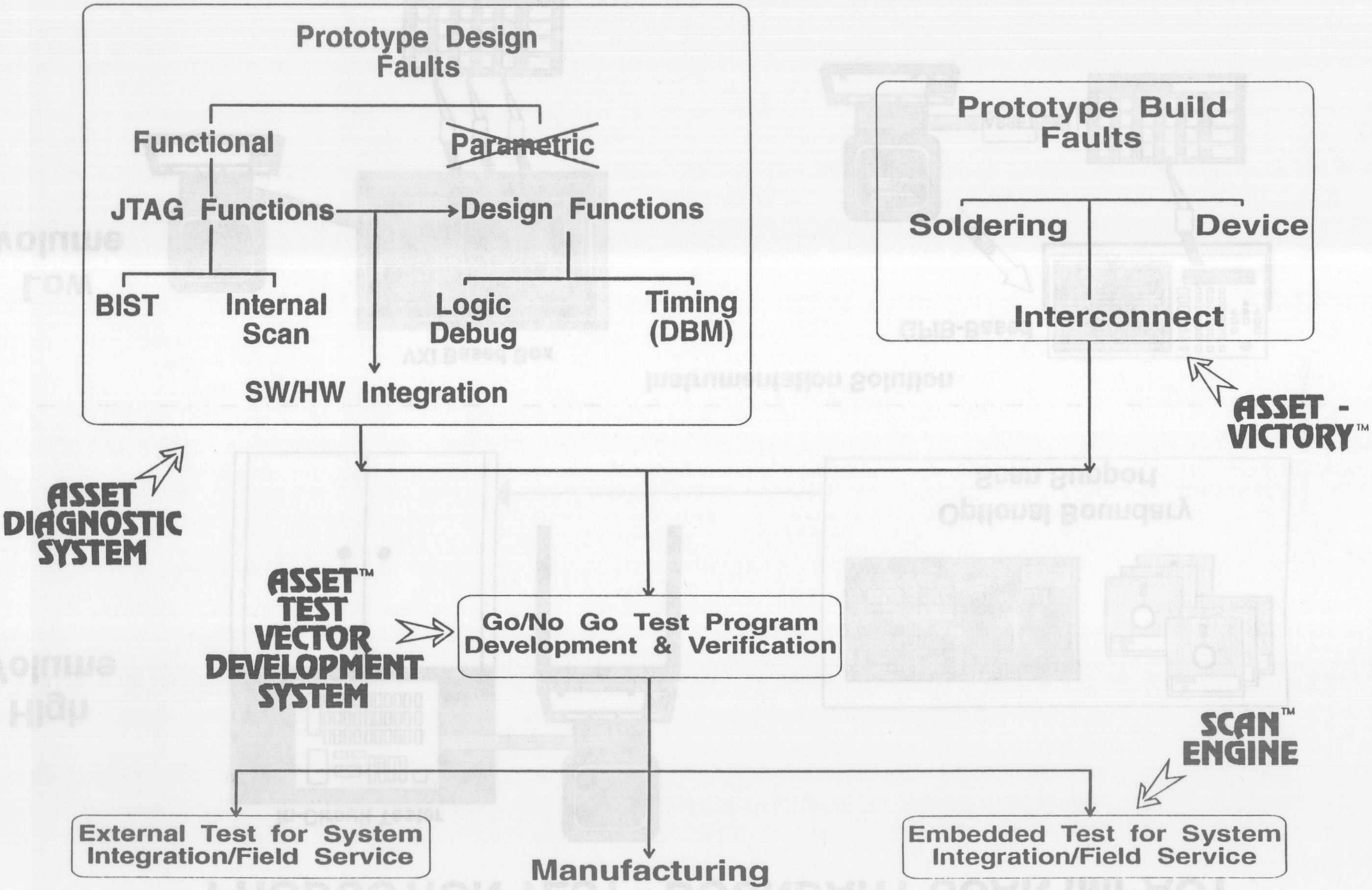
SYSTEM INTEGRATION & TEST
THREE ASSET APPLICATIONS



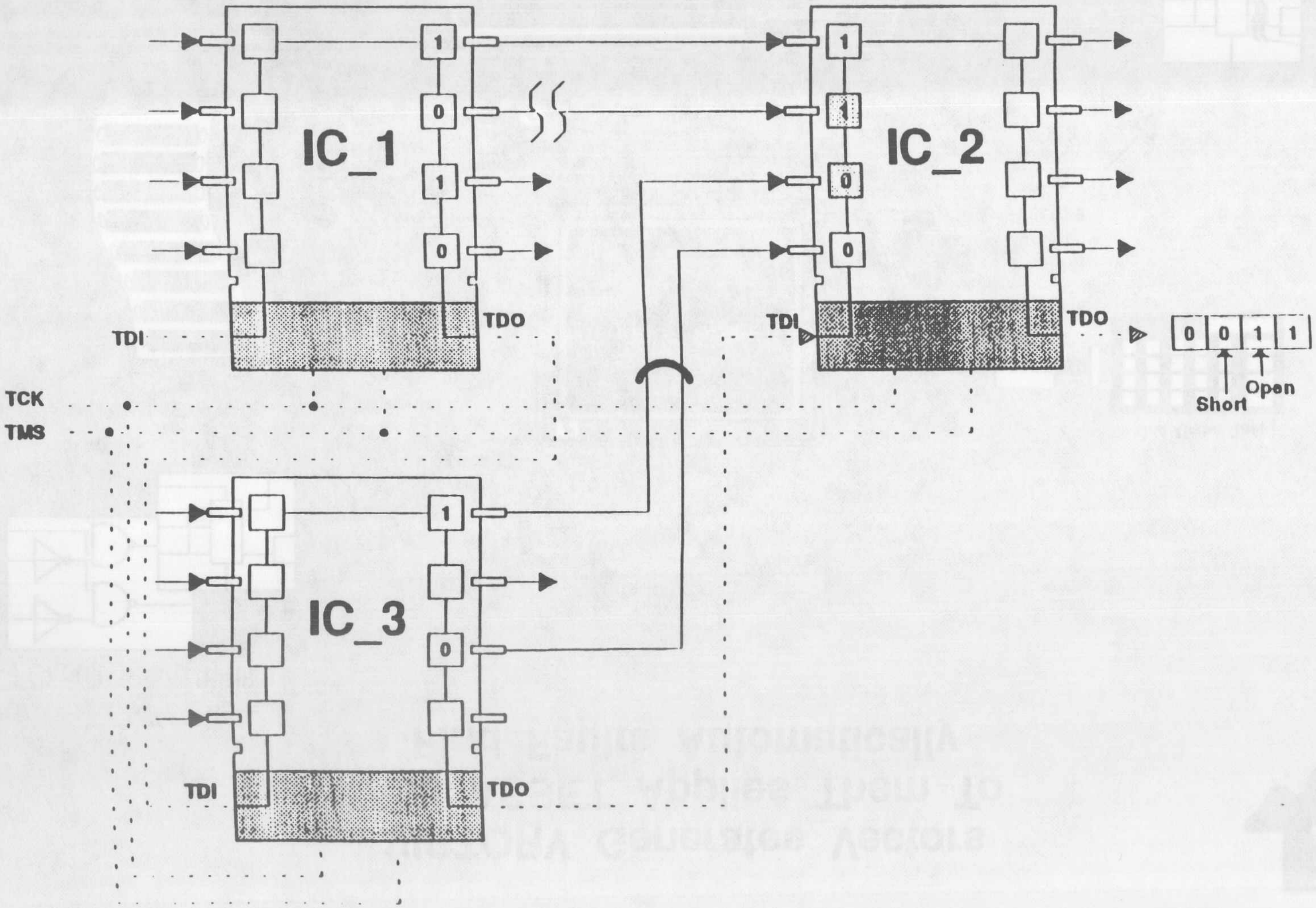
PRODUCTION TEST - BOUNDARY SCAN IMPACT



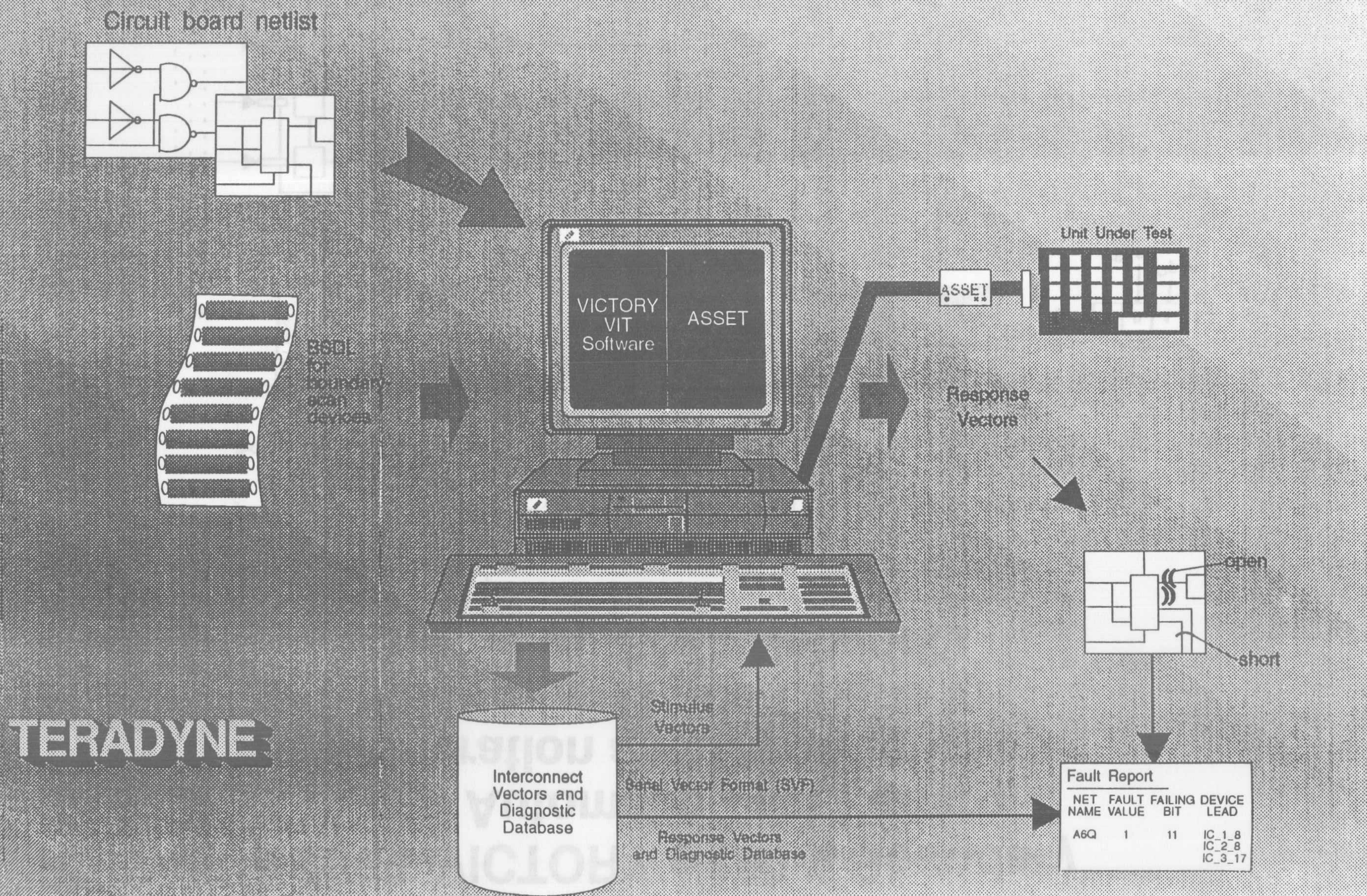
PROTOTYPE DIAGNOSTIC METHODOLOGY



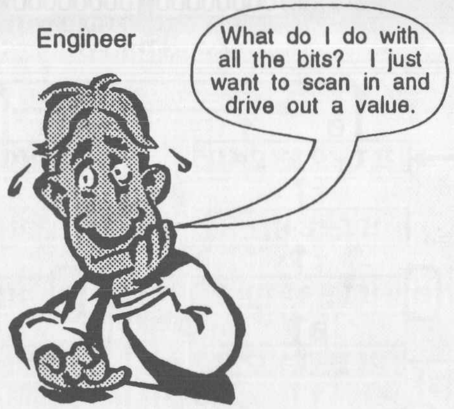
ASSET-VICTORY's 100% Boundary Scan Automatic Test Pattern Generation and Diagnostics: Finds Shorts and Opens in Boundary-Scan Networks



VICTORY Generates Vectors and ASSET Applies Them To Find Faults Automatically



ASSET SIMPLIFIES SCAN PATH MANAGEMENT . . .



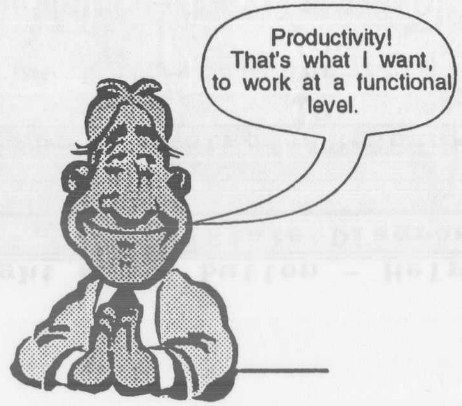
TAP MODE:

TDI	100010101 . . .
TDO	000001000 . . .
TMS	10100000 . . .
TCK	10101010 . . .

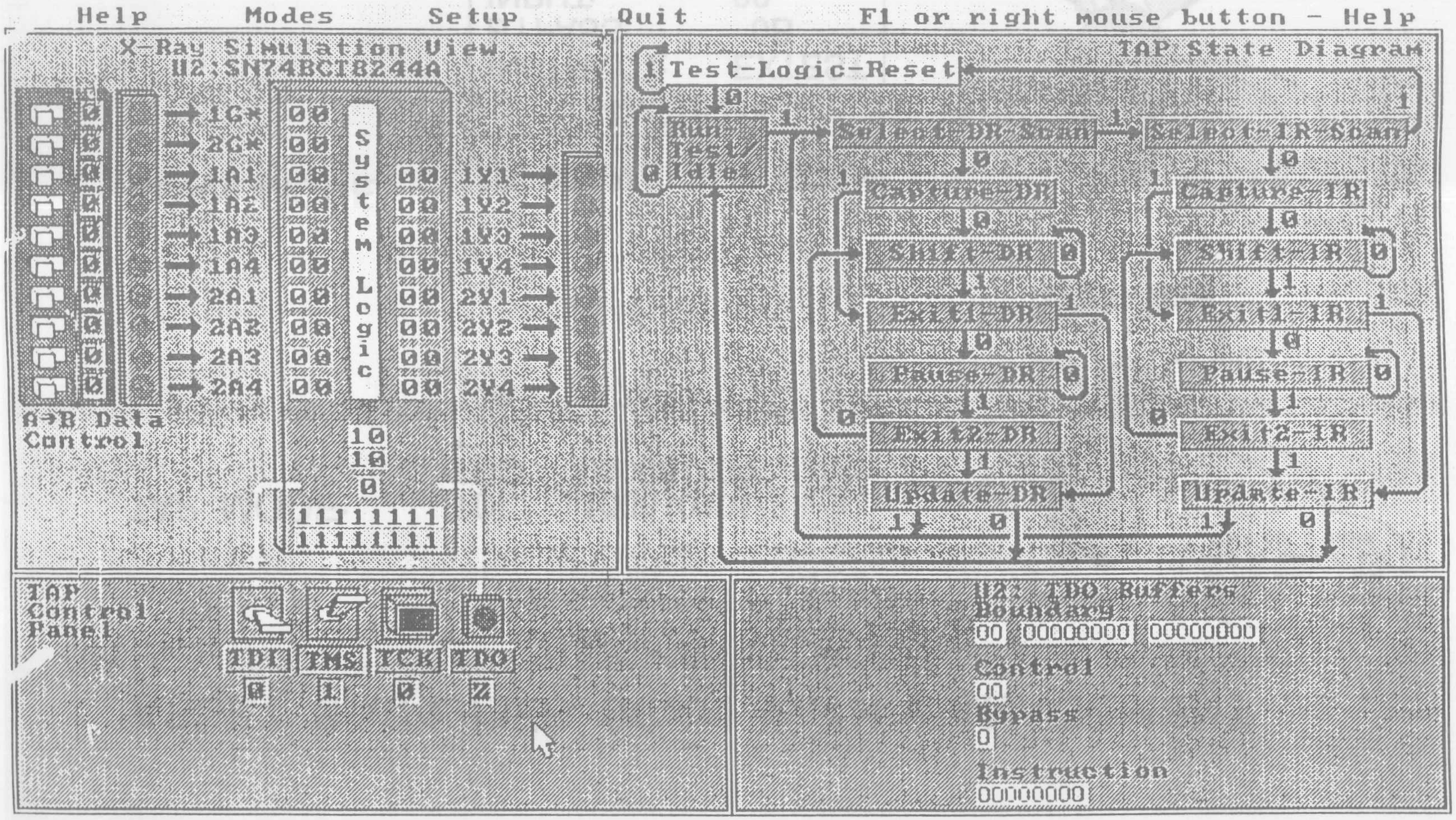
SCAN MODE: IR SCAN | DR SCAN

74ACT8244

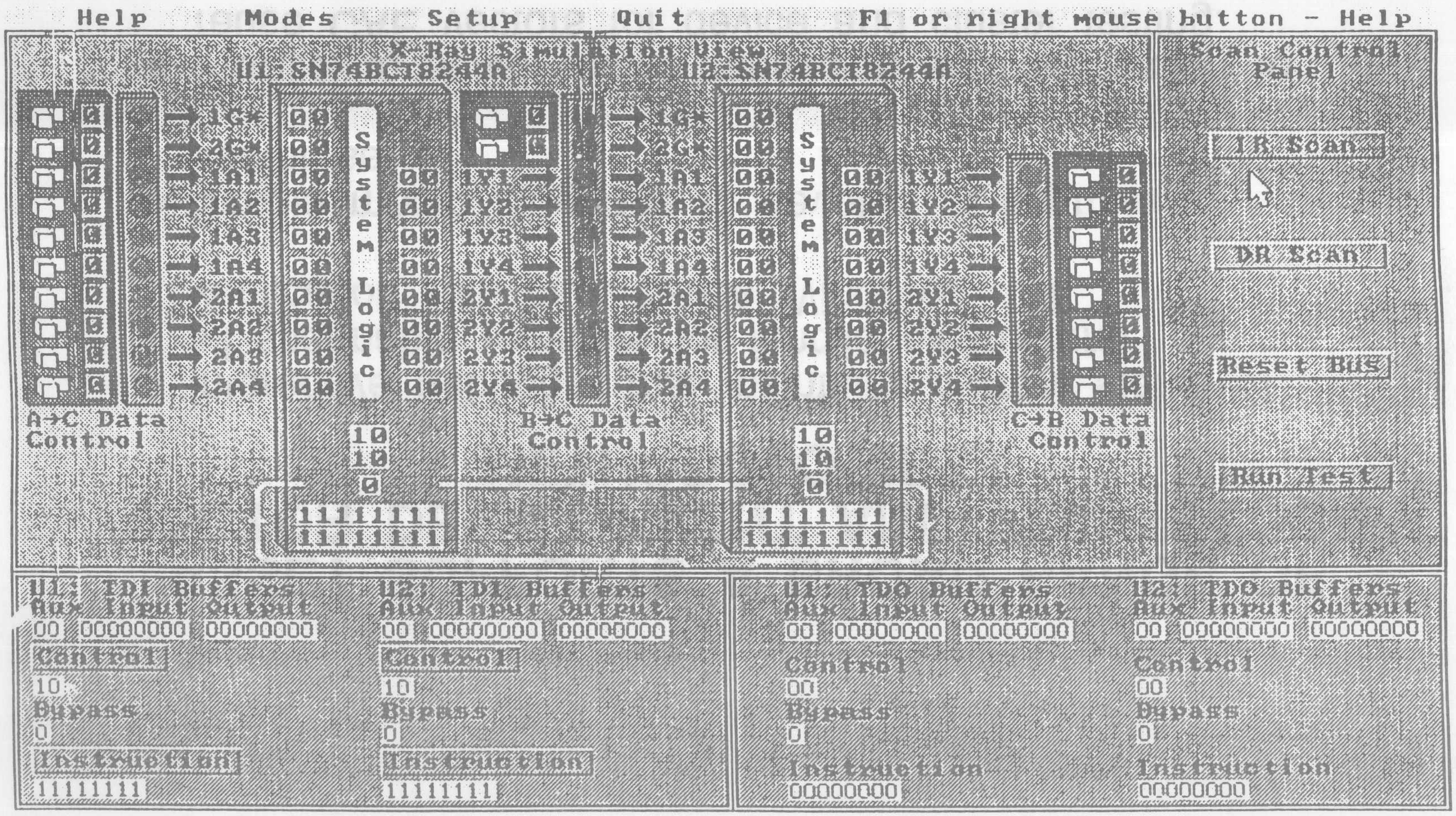
INSTRUCT:	EXTEST
BYPASS:	0B
INPUT:	00
OUTPUT:	A4H



TAP CONTROL MODE



SCAN CONTROL MODE



ASSET SUPPORTS A BROAD RANGE OF VECTOR DEVELOPMENT AND VERIFICATION METHODOLOGIES...

- Interactive debugger that maintains current status of all scannable registers for functional/structural verification with easy-to-use Windows U/I.

- Simple macro language to develop or improve a vector set.

- Parallel to serial vector translation and application to reuse CAE vectors for device and cluster testing.

- Serial vector input and applications through industry standard format - SVF.

ASSET SUPPORTS A BROAD RANGE OF VECTOR DEVELOPMENT AND VERIFICATION METHODOLOGIES...

- Virtual Interconnect ATPG using Teradyne's VIT product and ASSET.
- Test program development utilizing standard C++ and ASSET Scan Function Library.
- Access and control of internal scan and BIST through multiple applications.
- Scan path ATPG with ASSET.

ASSET SUPPORTS A BROAD RANGE OF ANALYSIS AND DIAGNOSTIC CAPABILITIES . . . .

- Analyze serial vector responses with serial displayer (ties SVF stimulus to response).
- Debugger:
  - interactive response and compare capabilities
- Scan Analyzer:
  - digital waveform display of scan operations
  - state table display
  - triggering capability
  - sequencing of triggers capability
  - compare actual response to simulation responses

ASSET SUPPORTS A BROAD RANGE OF ANALYSIS AND DIAGNOSTIC CAPABILITIES . . . .

- Access Analyzer:
  - network analysis to aid in adding boundary scan nodes
- Interconnect diagnostics to the net-level using VIT and ASSET with fault coverage reporting.
- BSDL/HSDL diagnostics through ASSET scan path ATPG

ASSET EASILY INTEGRATES INTO YOUR PRODUCT DEVELOPMENT FLOW . . . .

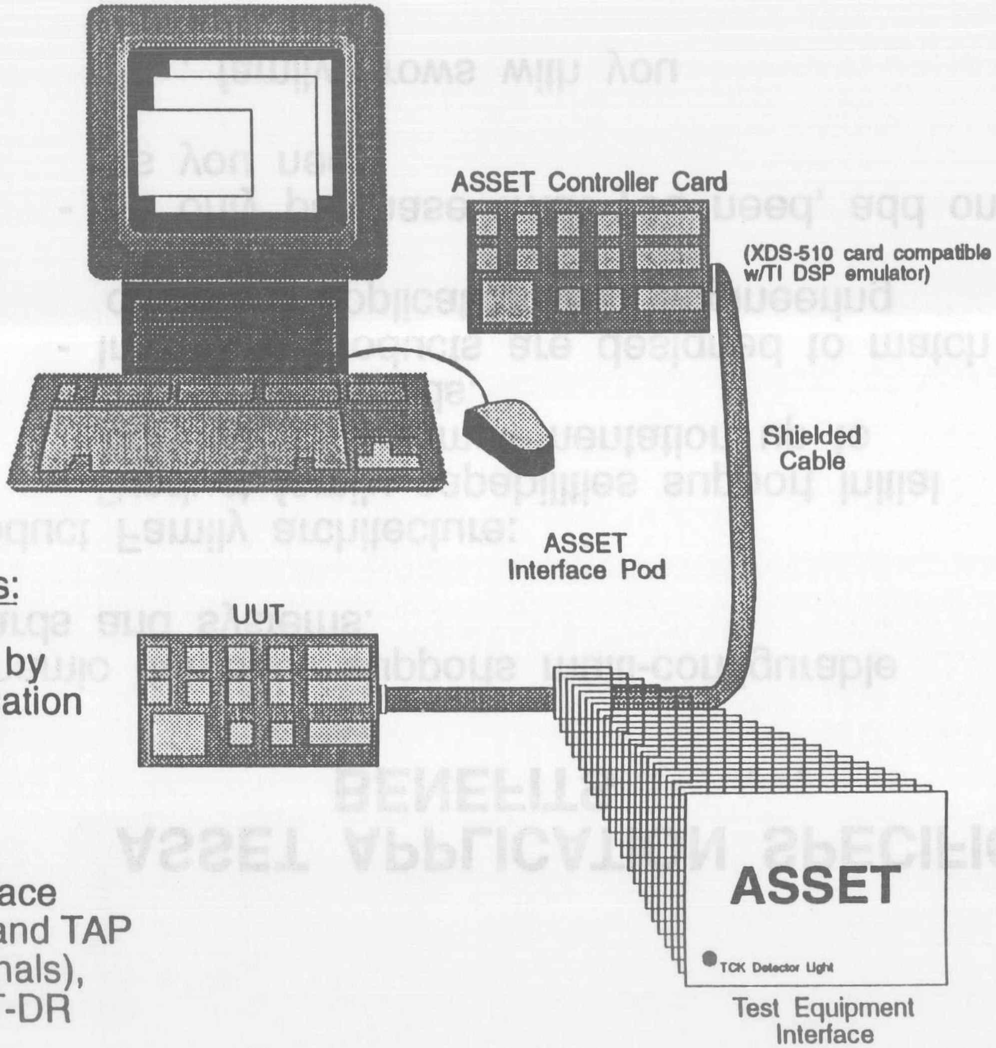
- CAE input:
  - TSSI
  - TDL
  - SVF
  - BSDL/HSDL
  - EDIF
- ATE output:
  - TSSI
  - SVF
  - re-use BSDL/HSDL
- Flow to embedded testability using Scan Engine and SVF.
- Integration with Tektronix for instrumentation.
- Flow to in-circuit testers with Teradyne

ASSET APPLICATION SPECIFIC BENEFITS . . . .

- Dynamic database supports multi-configurable boards and systems.
- Product Family architecture:
  - Product family capabilities support initial boundary-scan implementation up to 100% BS boards.
  - Individual products are designed to match customer application and engineering disciplines
  - So only purchase what you need, add only as you need

  . . . family grows with you

ASSET SYSTEM HARDWARE



Included in:
- ASSET Diagnostic System
- ASSET Test Vector System

Boundary Scan Signals:

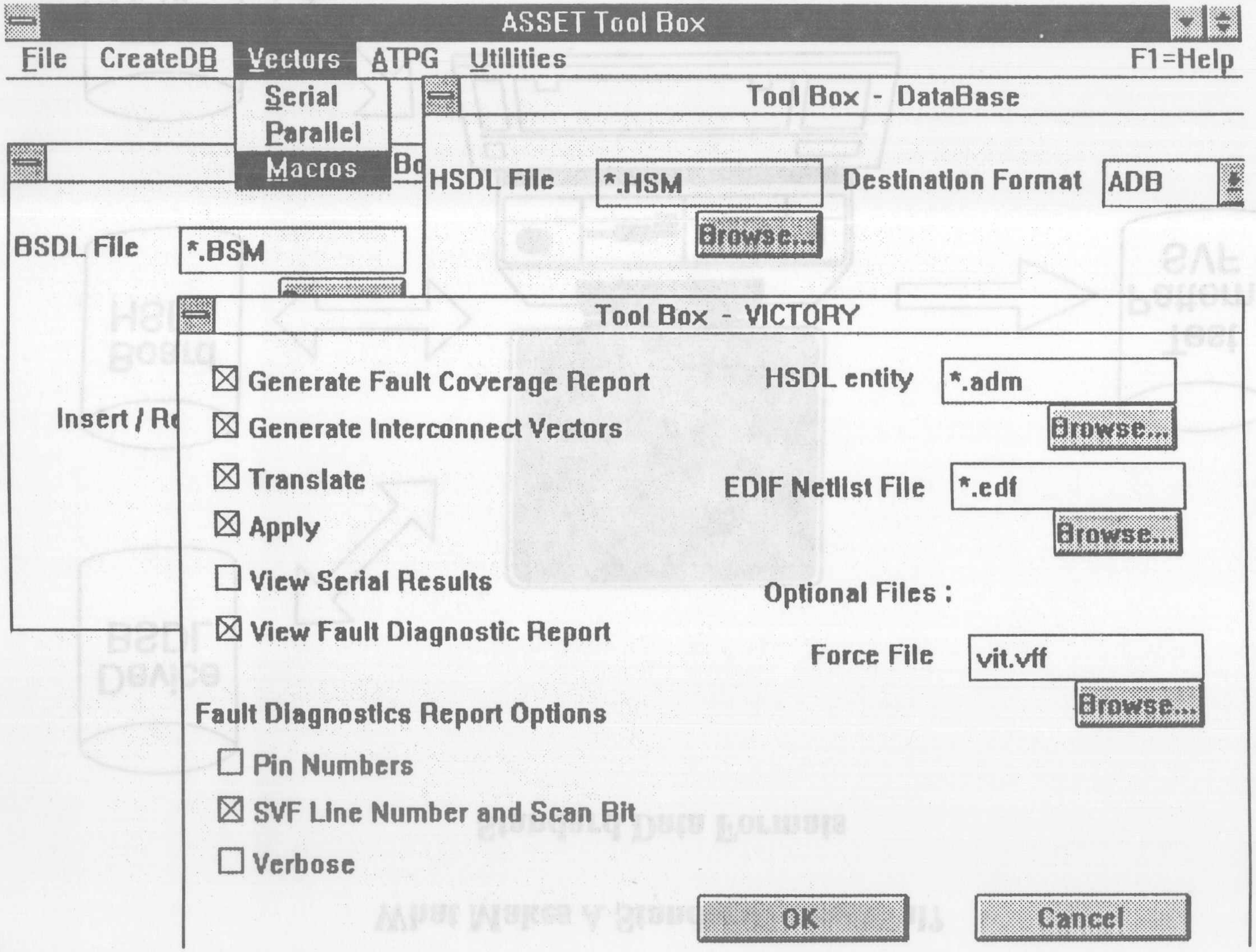
- TCK, TDO are driven by UUT (100 ohm termination or a single TTL load)
- TDI, TMS, and TRST driven by Pod

- Test Equipment Interface provides TCK, TMS, and TAP decoder output (4 signals), plus SHIFT-IR, SHIFT-DR CLK signals

Other Signals:

- programmable clock
  MAX: 20 MHz
  MIN: 1 MHz
- parallel I/O
  - 4 input
  - 4 output
- event qualification for at-speed tests
  - 2 signals
- ASSET 1.x pinout compatible

TEST VECTOR DEVELOPMENT SYSTEM



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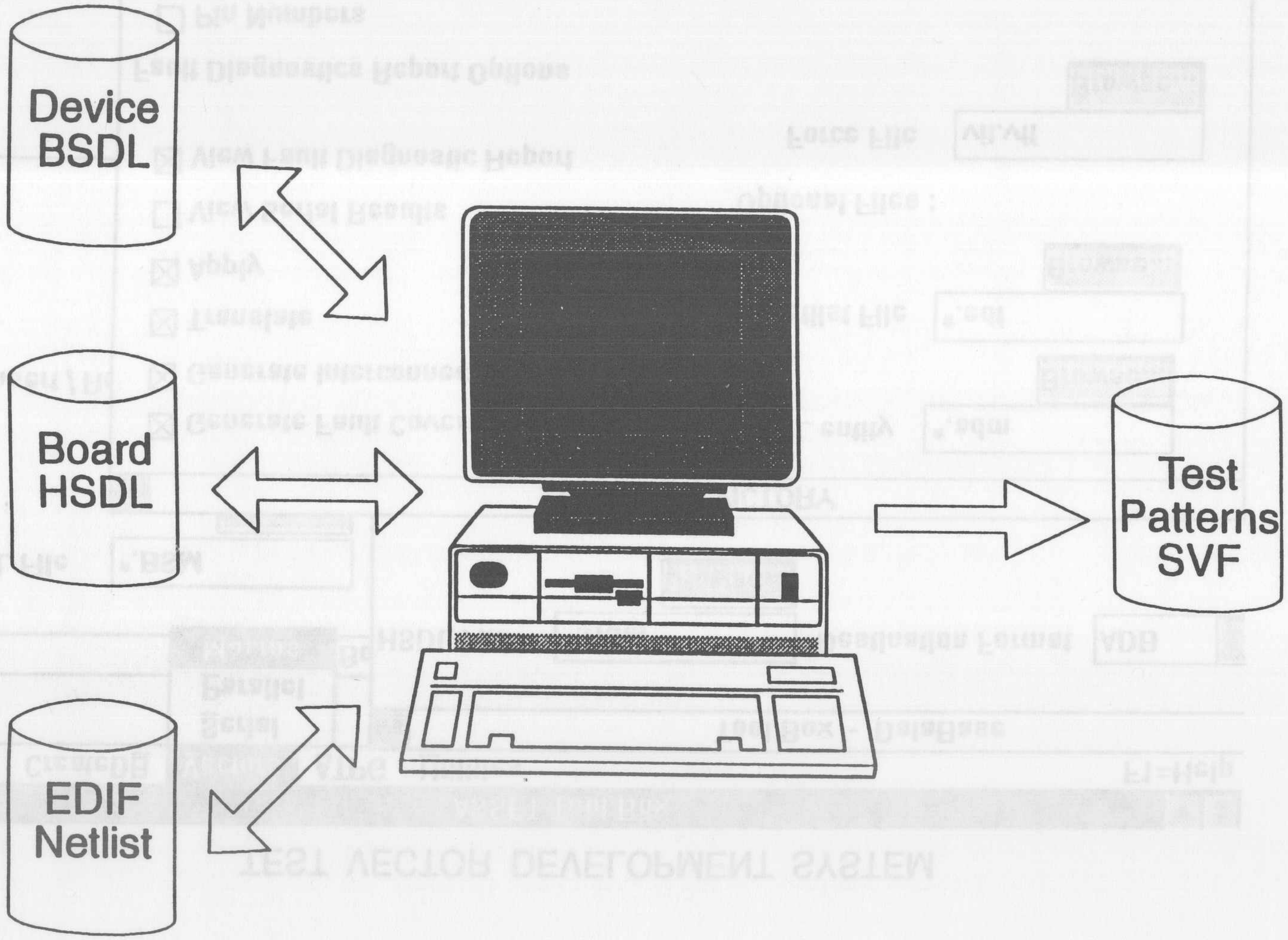
What Makes A Standard Successful?

Standard Data Formats



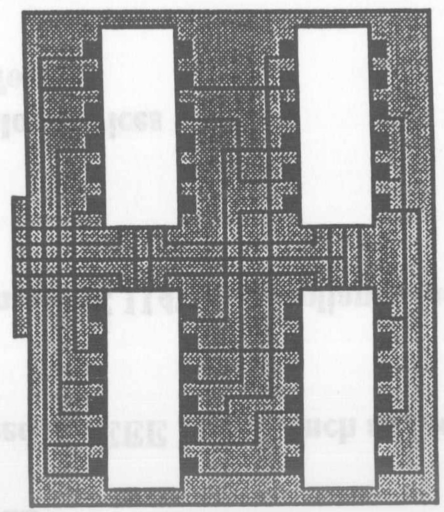
Standards Support and Development

BSDL - Boundary-Scan Description Language - BSDL is a language to describe the topology and characterisitcs of the ANSI/IEEE 1149.1 compliant circuitry designed into a device.

HSDL - Heirarchical-Scan Description Language - HSDL is a language to describe the topology and characteristics of the ANSI/IEEE 1149.1 compliant devices designed onto a board, module, system, multi-chip module.

BSDL for Device

HSDL for Board



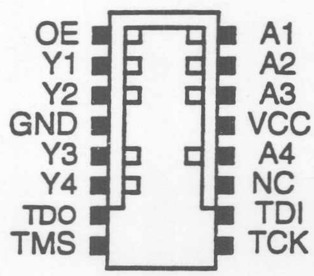
SVF - Serial Vector Format - SVF is a test vector representation that describes ANSI/IEEE 1149.1 transactions in terms of Test Access Port (TAP) behavior. SVF raises the level of abstration to human readable efficient format which is independent of any controller device.

BSDL

- BSDL is a data description format that tools may read
- BSDL descriptions exclude anything explicitly defined in IEEE 1149.1, such as the Test Access Port (TAP) state transitions
- Proposed uses include: test generation and execution, IEEE 1149.1 compliance monitoring/checking, as a front-end to synthesis of IEEE 1149.1 devices
- TI endorses BSDL and offer support by:
  TI will provide BSDL files for TI's standard catalog devices
  TI's ASSET tool supports BSDL as a data input format
- TI will make BSDL files available through:
  1) Bulletin board down-load via modem
  2) Through TI field sales or authorized distributors
- To complement BSDL, TI is developing a language for describing boards, modules, systems, multi-chip modules, and internals of devices. The language is Heirarchical-Scan Description Language (HSDL). A copy of the HSDL specification contact the Test Technology Center at (214) 575-2577.

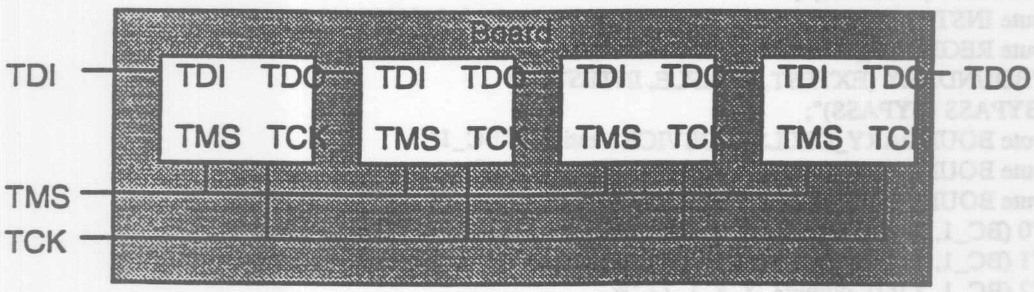
Example BSDL Device Description (abbreviated)

```
entity DEVICE is
    generic (PHYSICAL_PIN_MAP : string : = "UNDEFINED");
    port (OE_NEG1:in bit;
        Y1:out bit_vector(1 to 4);
        A1:in bit_vector (1 to 4);
        GND, VCC, NC:linkage bit;
        TDO:out bit;
        TDI, TMS, TCK:in bit);
    use STD_1149.1_1990.all
    attribute PIN_MAP of DEVICE : entity is PHYSICAL_PIN_MAP;
    constant XX_PACKAGE : PIN_MAP_STRING : = "OE_NEG1:1, Y1:(2,3,4,5), A1:(6,7,8,9), GND:10,"&
                                             "VCC:11, TDO:12, TDI:13, TMS:14, TCK:15,"&
                                             "NC:16";
    attribute TAP_SCAN_IN of TDI : signal is true;
    attribute TAP_SCAN_MODE of TMS : signal is true;
    attribute TAP_SCAN_OUT of TDO : signal is true;
    attribute TAP_SCAN_CLOCK of TCK: signal is (20.0e6, BOTH);
    attribute INSTRUCTION_LENGTH of DEVICE : entity is 8;
    attribute INSTRUCTION_OPCODE of DEVICE : entity is
        "EXTEST (00000000),"&
        "BYPASS (11111111),"&
        "SAMPLE (00000010),"&
        "INTEST (00000011)";
    attribute INSTRUCTION_CAPTURE of DEVICE : entity is "10000001";
    attribute REGISTER_ACCESS of DEVICE : entity is
        "BOUNDARY (EXTEST, SAMPLE, INTEST),"&
        BYPASS (BYPASS)";
    attribute BOUNDARY_CELLS of DEVICE : entity is "BC_1";
    attribute BOUNDARY_LENGTH of DEVICE : entity is 9;
    attribute BOUNDARY_REGISTER of DEVICE : entity is
        "0 (BC_1, Y1(4), output3, X, 8, 1, Z),"&
        "1 (BC_1, Y1(3), output3, X, 8, 1, Z),"&
        "2 (BC_1, Y1(2), output3, X, 8, 1, Z),"&
        "3 (BC_1, Y1(1), output3, X, 8, 1, Z),"&
        "4 (BC_1, A1(4), input, X),"&
        "5 (BC_1, A1(3), input, X),"&
        "6 (BC_1, A1(2), input, X),"&
        "7 (BC_1, A1(1), input, X),"&
        "8 (BC_1, * ,control, 1)";
end DEVICE;
```



Example HSDL Board Description

```
entity BOARD is
    attribute (PHYSICAL_PIN_MAP : string : = "UNDEFINED");
    port (TCK :in bit;
        TDO :out bit;
        TMS, TDI :in bit);
    use STD_1149.1_1990.all;
    use HSDL_module.all;
    attribute MODULE_DESCRIPTION of BOARD is
        "The board is an example board that was created from Figure 3-1 of IEEE 1149.1-1990 Specification";
    attribute PIN_MAP of BOARD : entity is PHYSICAL_PIN_MAP;
    constant ONLY_PACKAGE : PIN_MAP_STRING : = "TDI:J1, TDO:J2, TCK:J3, TMS:J4";
    attribute TAP_SCAN_IN of TDI : signal is true;
    attribute TAP_SCAN_MODE of TMS : signal is true;
    attribute TAP_SCAN_OUT of TDO : signal is true;
    attribute TAP_SCAN_CLOCK of TCK: signal is (20.0e6, BOTH);
    attribute MEMBERS of BOARD : entity is
        "U1 (DEVICE1, FK),"&
        "U2 (DEVICE2, NT),"&
        "U3 (DEVICE3, FN),"&
        "U4 (DEVICE4, JT)";
    constant PATH : STATIC_PATH : = "U1, U2, U3, U4";
end BOARD;
```



KEY HSDL FEATURES NETLIST'S DO NOT SUPPORT

☞ **Different scan path types for system design**
- static paths
- dynamic paths (path switching)
- external paths (re-configurable systems)

☞ **Interactive capabilities to ease use**
- symbol (mnemonic) support
  - registers (PSA vs. 01)
  - buses (SN74ABT8373 vs. 01010000....)
  - instructions (EXTEST vs. 00000000)
- composition support
  - register (concatenate multiple test reg)
  - buses (32-bit ADDR bus, concatenation of 4 octals)
- register capture (for bypass 1-passes, 0-fails)

☞ **Prevention of illegal conditions**
- contraints (bus conflicts)

Serial Vector Format (SVF)

What is SVF?

SVF describes ANSI/IEEE 1149.1 transactions in terms of test access access port (TAP) behavior

SVF raises the level of abstraction to human readable, efficient format which is independent of any controller device

Features of SVF

- ASCII
- Transmit, Receive, Mask data aligned
- Describes bus activity as transitions to stable states
- Supports "Vector Offsets" for re-usability, efficiency
- Describes synchronous parallel I/O
- Easily translatable

How to get a copy of SVF specification?

Contact Texas Instruments:

Texas Instruments
6500 Chase Oaks Blvd.
M/S 8407
Plano, TX 75023
attn: Doug Kostlan

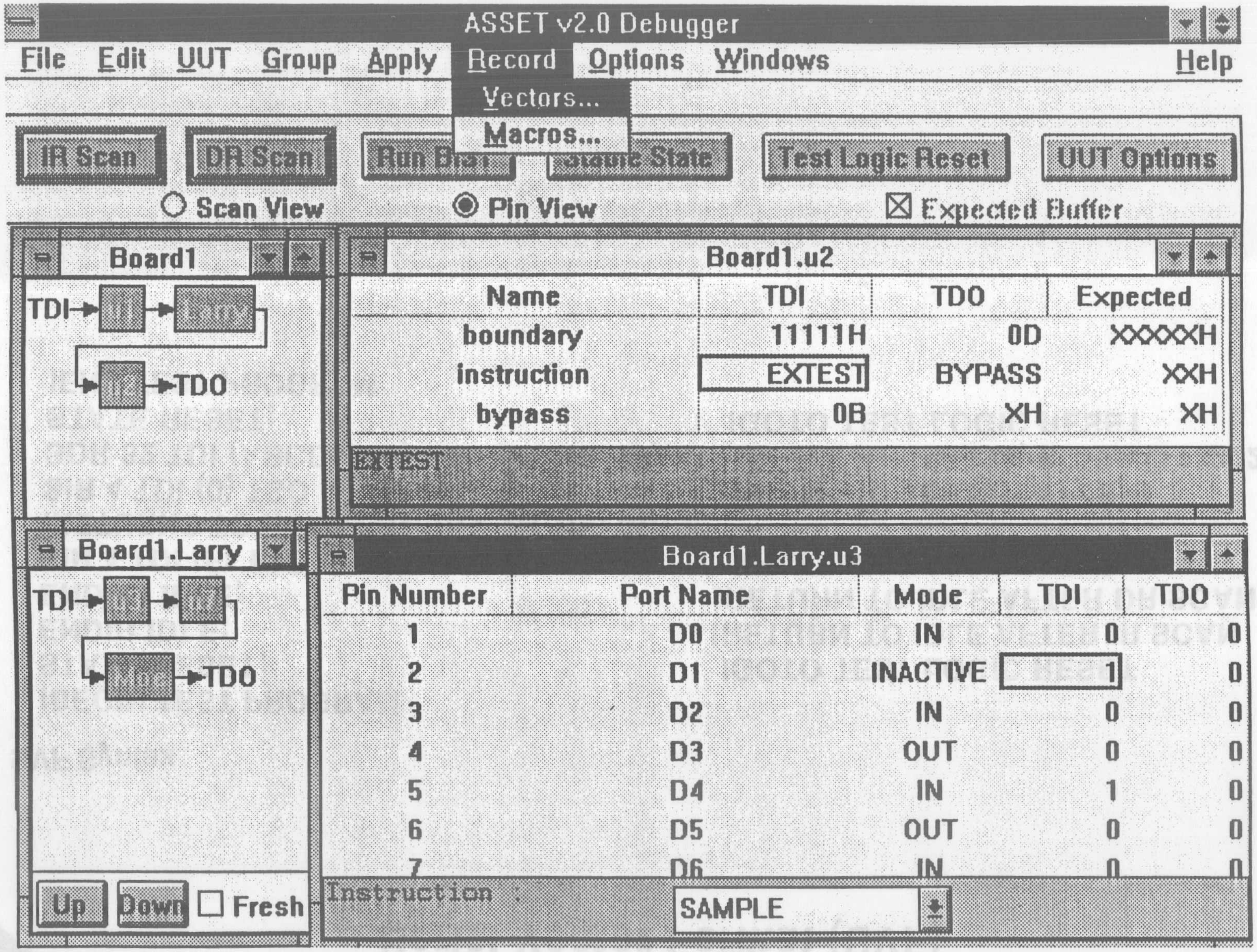
or 214-575-3722 (phone)
214-575-6198 (fax)

Serial Vector Format (SVF)

SVF Syntax

```
!BEGIN TEST PROGRAM
STATE RESET;                                  !GOTO TEST LOGIC RESET
ENDIR IDLE;                                   !RETURN TO IDLE AFTER IR SCAN
ENDDR IDLE;                                   !RETURN TO IDLE AFTER DR SCAN
SIR 4 TDI (F) TDO (9) MASK (F);               !INSTR=BYPASS,STATUS=9
!RETURNS TO RUN-TEST/IDLE BY DEFAULT
SIR 4 TDI (0) TSO (9) MASK (F);               !INSTR=EXTEST,STATUS=9
SDR 32 TDI (ABCD1234) TDO (11112222);         !DRIVE ABCD1234, RCV=11112222
STATE RESET;                                  !GOTO TEST LOGIC RESET
!END TEST PROGRAM
```

DIAGNOSTIC SYSTEM - DEBUGGER APPLICATION



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SCAN FUNCTION LIBRARY

Scan Functions

sc - clk
sc - illegal-chk
sc - iord
sc - iow
sc - run
sc - scan
sc - sethier
sc - state
sc - stimulate
sc - strap
sc - connect
"
"

User-Interface

- ASSET 1.x - 2.0 upgrade compatible

- MS Windows compatible U/I library of functions

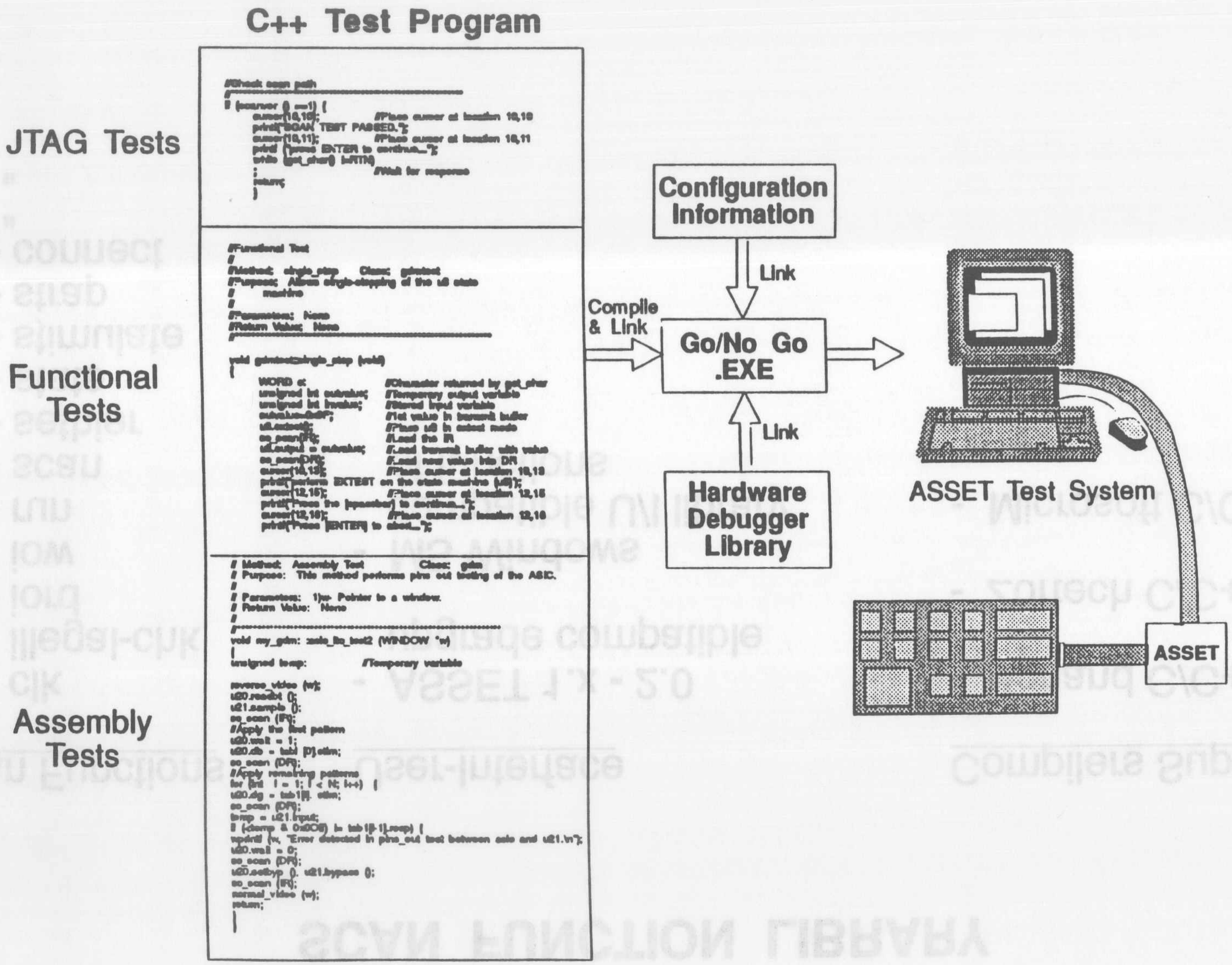
Compilers Supported:

- Borland C/C++

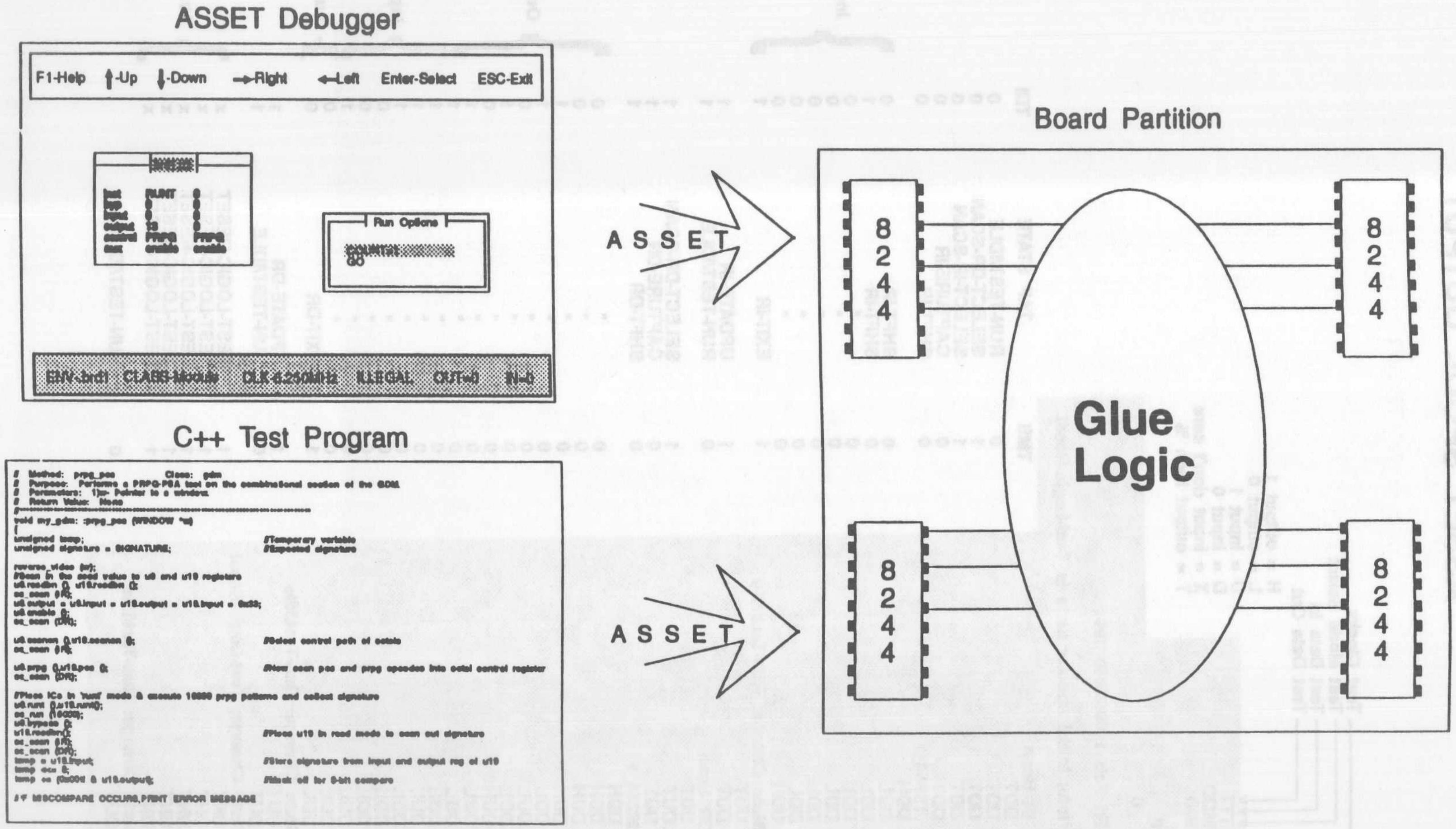
- Zortech C/C++

- Microsoft C/C++

ASSET SCAN FUNCTION LIBRARY



ASSET/OCTAL APPLICATION - BIST



ASSET SPOOL OUTPUT

Test Clocks
Test Mode Select
Test Data In
Test Data Out

H = output 1
L = output 0
U = input 1
D = input 0
X = input don't care
T = output high %

```
# TTT
# MDD
# SIO
#
# II
#   0
#
# Fri Feb 1 09:48:40 1991
#
# Note: Initial spooler state is Test-Logic-Reset
#
#  IR Scan
0  DDT
1  UDT
2  UDT
3  DDT
4  DDT
$  .T8244_1
5  DDH
6  DUL
7  DDL
8  DDL
9  DDL
10 DDL
11 DDL
12 UUH
# State Change: Run-Test/Idle
13 UUT
14 DUT
# DR Scan
15 UUT
16 DUT
17 DUT
# .t8244_1
18 DDH
19 DDH
20 DUH
21 DUH
22 DDL
23 DUL
24 DDL
25 DUH
26 DUL
27 DUL
28 DUL
29 DUL
30 DDL
31 DDL
32 DDL
33 DUL
34 DUL
35 UDL
# State Change: Run-Test/Idle
36 UUT
37 DUT
# State Change: Test-Logic-Reset
38 UNT
39 UNT
40 UNT
41 UNT
42 UNT
# State Change: Run-Test/Idle
43 DUT
```

TMS	TAP STATE	TDI	
0	RUN-TEST/IDLE	0	
1	SELECT-DR-SCAN	0	
1	SELECT-IR-SCAN	0	
0	CAPTURE-IR	0	
0	SHFT-IR	0	
0	SHFT-IR	0	Instruction = sample 82
0	SHFT-IR	1	
0	·	0	
0	·	0	
0	·	0	
0	·	0	
0	·	0	
1	EXIT-IR	1	
1	UPDATE-IR	1	
0	RUN-TEST/IDLE	1	
1	SELECT-DR-SCAN	1	
0	CAPTURE-DR	1	
0	SHFT-DR	1	
0	·	0	Output = 35
0	·	0	
0	·	1	
0	·	1	
0	·	0	
0	·	1	
0	·	0	
0	·	1	
0	·	1	Input = F1
0	·	1	
0	·	1	
0	·	1	
0	·	0	
0	·	0	
0	·	1	
0	·	0	Aux = 0
1	EXIT-DR	0	
1	UPDATE-DR	1	
0	RUN-TEST/IDLE	1	
1	TEST-LOGIC-RESET	x	Strap
1	TEST-LOGIC-RESET	x	
1	TEST-LOGIC-RESET	x	
1	TEST-LOGIC-RESET	x	
1	TEST-LOGIC-RESET	x	
0	RUN-TEST/IDLE		

TO ORDER ASSET

PRODUCT NAME	PART #
ASSET Diagnostic System	ASSET-DSYS-PC
ASSET Test Vector Development System	ASSET-TSYS-PC
Boundary Scan Demonstration Board	ASSET-BSDM-PC
General Demonstration Board	ASSET-GDM-PC
Scan Function Library	ASSET-SLIB-PC

* Contact TI Sales Office or TI Authorized Distributor

NOTES